In-Class Homework for Module 1 – No. 1
Wednesday, January 15, 2014

Given the truth table, below, determine the following:

X	Y	Z	F(X,Y,Z)
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

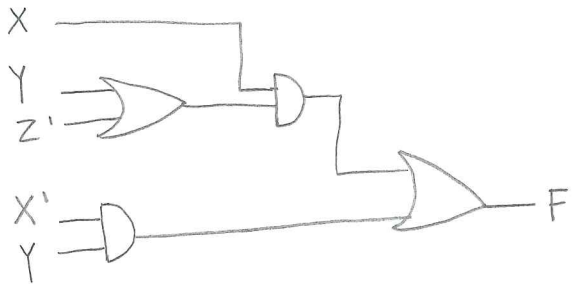
Truth tables for the *dual* $F^D(X,Y,Z)$ and *complement* $F'(X,Y,Z)$ functions:

X	Y	Z	$F^D(X,Y,Z)$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

X	Y	Z	$F'(X,Y,Z)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

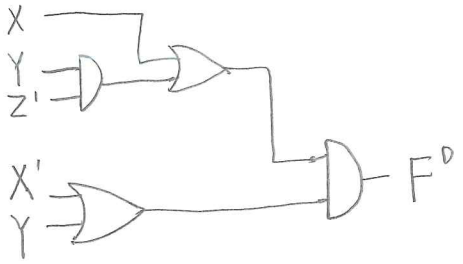
Practice finding dual and complement functions/circuit realizations:

F(X,Y,Z) = X•(Y+Z') + X'•Y



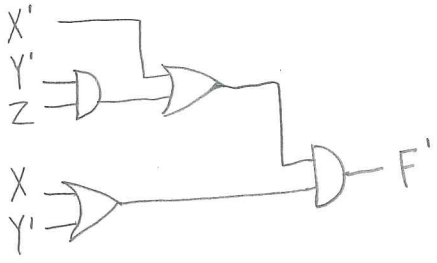
F^D(X,Y,Z) the DUAL of function F, above

$F^D(X,Y,Z) = (X + (Y \cdot Z')) \cdot (X' + Y)$



F'(X,Y,Z) the COMPLEMENT of function F, above

$F'(X,Y,Z) = (X' + (Y' \cdot Z)) \cdot (X + Y')$



In-Class Homework for Module 1 – No. 2
Friday, January 17, 2014

1. Write a formula for OHM's LAW:

   $V = I \times R$

2. Write a formula for POWER:

   $P = V_{drop} \times I$

3. Describe what a resistor does:

   Limits the amount of current flowing through a circuit

4. Describe the functionality of a MOSFET:

   - Voltage controlled impedance
   - Used to construct CMOS devices

5. A functional difference between an N-channel MOSFET and a P-channel MOSFET is:

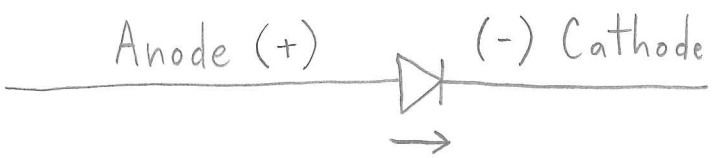
   N-channel MOSFET

   When v_{in} is high (transistor is turned on), v_{out} is low. When v_{in} is low, the transistor is turned off.

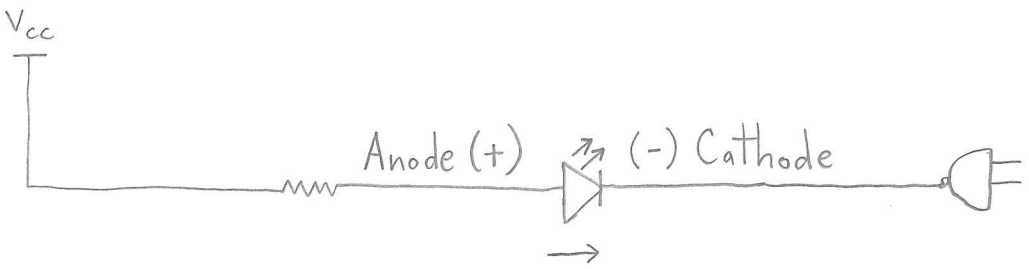
   P-channel MOSFET

   When v_{in} is low (transistor is turned on), v_{out} is high. When v_{in} is high, the transistor is turned off.

6. Draw a symbol of a diode, label its terminals, and include the current arrow for a forward biased device.

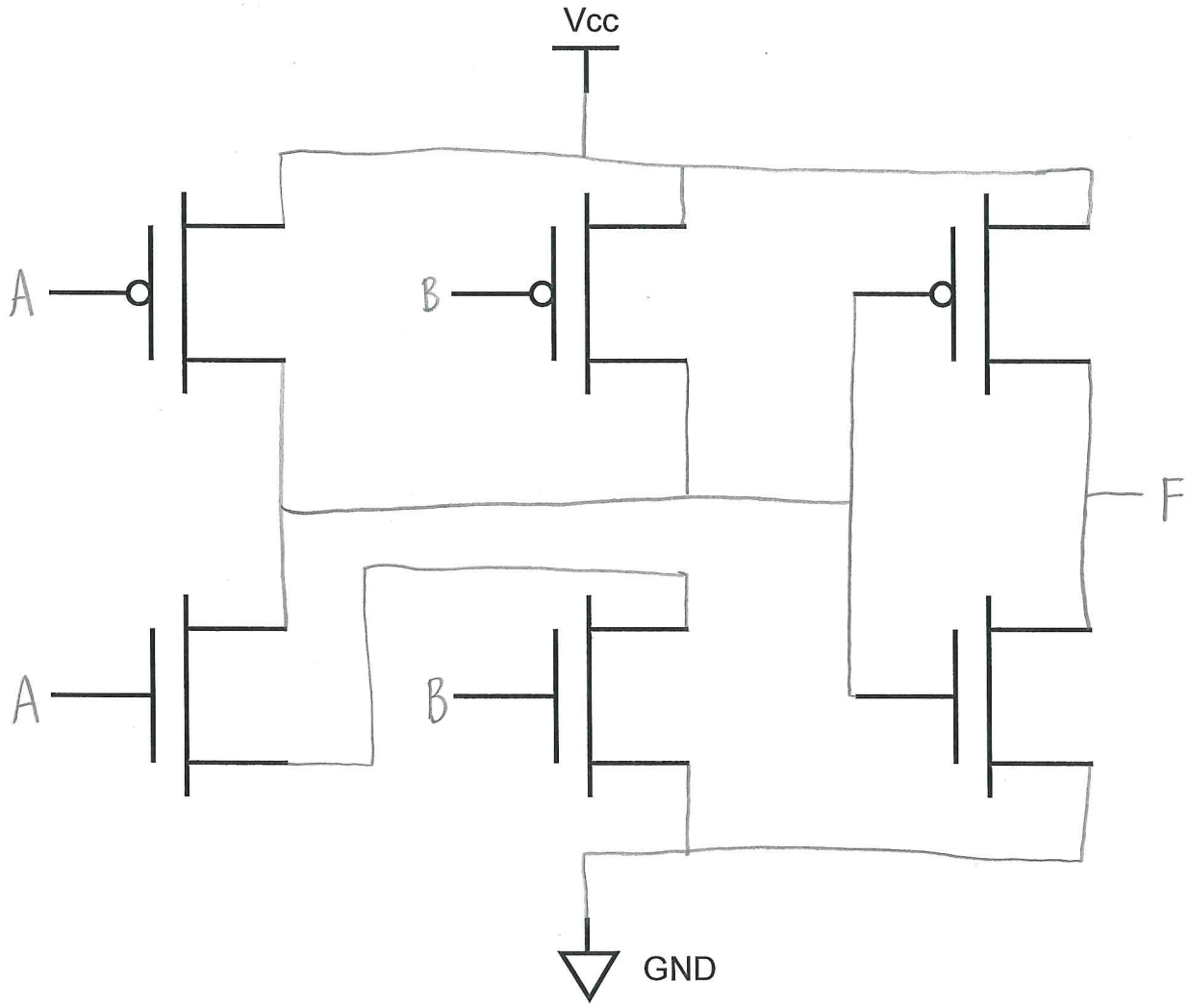


7. Draw a symbol of a Light Emitting Diode with a current limiting resistor, label its terminals, and include the current arrow for a forward biased device.

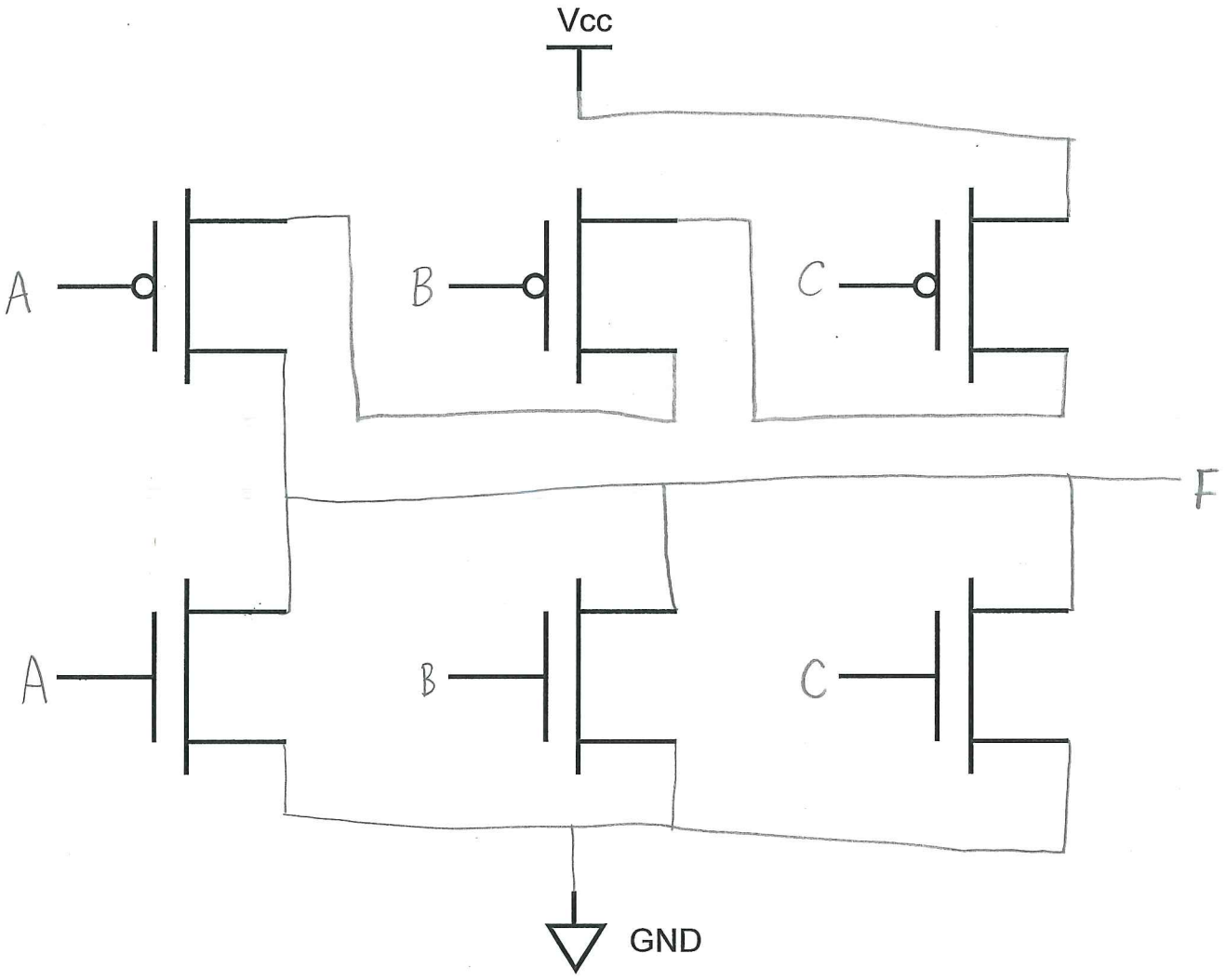


In-Class Homework for Module 1 – No. 3
Wednesday, January 22, 2014

1. Using a total of **three** N-channel MOSFETs and **three** P-channel MOSFETs, draw a circuit schematic for a **two-input AND** gate. The gate inputs should be labeled A and B, and the gate output should be labeled F. Be sure to show the power (Vcc) and ground (GND) connections as well.



2. Using a total of **three** N-channel MOSFETs and **three** P-channel MOSFETs, draw a circuit schematic for a **three-input NOR** gate. The gate inputs should be labeled A, B, C and the gate output should be labeled F. Be sure to show the power (Vcc) and ground (GND) connections as well.



In-Class Homework for Module 1 – No. 4
Monday, January 27, 2014

Assume two hypothetical logic families have the following D.C. characteristics:

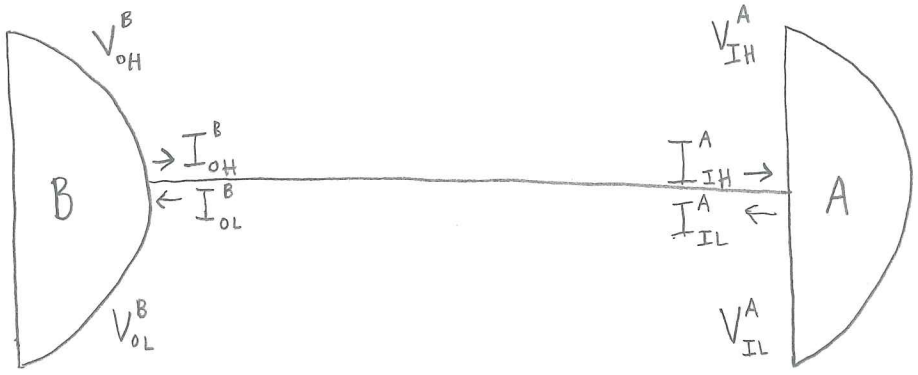
Logic Family "A"

$V_{CC} = 5$ V	$V_{OH} = 3.50$ V	$V_{OL} = 0.50$ V	$V_{IH} = 2.50$ V	$V_{IL} = 1.00$ V
$V_{TH} = (V_{OH} - V_{OL})/2$	$I_{OH} = -500$ µA	$I_{OL} = 10$ mA	$I_{IH} = 50$ µA	$I_{IL} = -1.5$ mA

Logic Family "B"

$V_{CC} = 5$ V	$V_{OH} = 4.50$ V	$V_{OL} = 0.5$ V	$V_{IH} = 3.00$ V	$V_{IL} = 1.50$ V
$V_{TH} = (V_{OH} - V_{OL})/2$	$I_{OH} = -5$ mA	$I_{OL} = 10$ mA	$I_{IH} = 0.5$ µA	$I_{IL} = -0.5$ µA

Can gates from family "B" be used to drive gates from family "A"? Explain your answer by calculating and considering fan-out and DC noise margin.



Fanout $_{B\to A}$ = $\min\left(\frac{I_{OH}^B}{I_{IH}^A}, \frac{I_{OL}^B}{I_{IL}^A}\right) = \min\left(\frac{5\times10^{-3}}{5\times10^{-5}}, \frac{10\times10^{-3}}{1.5\times10^{-3}}\right) \approx 6.7$ Practical fanout is $\underline{6}$.

DCNM $_{B\to A}$ = $\min\left(V_{OH}^B - V_{IH}^A, V_{IL}^A - V_{OL}^B\right) = \min(4.5V - 2.5V, 1.0V - 0.5V) = 0.5V$

Conclusion: Because the fanout is ≥1 and DCNM is > 0, gates from family "B" can drive gates from family "A".

Given that a (5-volt) CMOS gate's P-channel output pull-up has an "on" resistance of 100Ω and that its N-channel output pull-down has an "on" resistance of 50Ω:

(a) **If the desired V_{OHmin} is 4.5 volts and the desired V_{OLmax} is 0.5 volts, what are the gate's I_{OHmax} and I_{OLmax} ratings?**

$\frac{V_{CC}-V_{OHmin}}{R_p} = \frac{5V-4.5V}{100\Omega} = \frac{0.5V}{100\Omega} = 5mA$

$\frac{V_{OLmax}-V_{GND}}{R_n} = \frac{0.5V-0V}{50\Omega} = \frac{0.5V}{50\Omega} = 10mA$

I_{OHmax} = 5 mA I_{OLmax} = 10 mA

(b) **If a DCNM of 1.5 volts is desired for this CMOS gate family, what do its V_{IHmin} and V_{ILmax} specifications need to be, based on the values given in part (a)?**

$DCNM = V_{OHmin} - V_{IHmin}$

$V_{IHmin} = V_{OHmin} - DCNM$

$= 4.5V - 1.5V$

$= 3.0\ V$

V_{IHmin} = 3.0 V

$DCNM = V_{ILmax} - V_{OLmax}$

$DCNM + V_{OLmax} = V_{ILmax}$

$1.5V + 0.5V =$

$2.0V =$

V_{ILmax} = 2.0 V

(c) **If the I_{IH} and I_{IL} specifications for gates in this family are +0.1 mA and -0.1 mA, respectively, what is the practical fan-out for circuits constructed using these gates, based on values calculated in part (a)?**

$\min\left(\frac{I_{OHmin}}{I_{IH}}, \frac{I_{OLmax}}{I_{IL}}\right) =$

$= \min\left(\frac{5mA}{0.1mA}, \frac{10mA}{0.1mA}\right)$

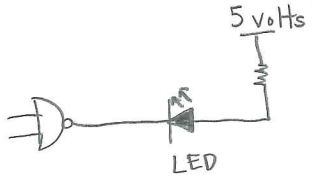
$= \min(50, 100)$

$= 50$

Practical fan-out = 50

(d) **Show how an LED (with forward voltage V_{LED} = 1.5 V) should be interfaced to gates in this family to obtain maximum brightness, and calculate the value of the current limiting resistor required along with its power dissipation.**

Circuit and calculations:



$R = \frac{V_{Total}}{I_{OLmax}} = \frac{V_{CC}-V_{OL}-V_{LED}}{I_{OLmax}} = \frac{5V-0.5V-1.5V}{10mA} = \frac{3V}{10mA}$

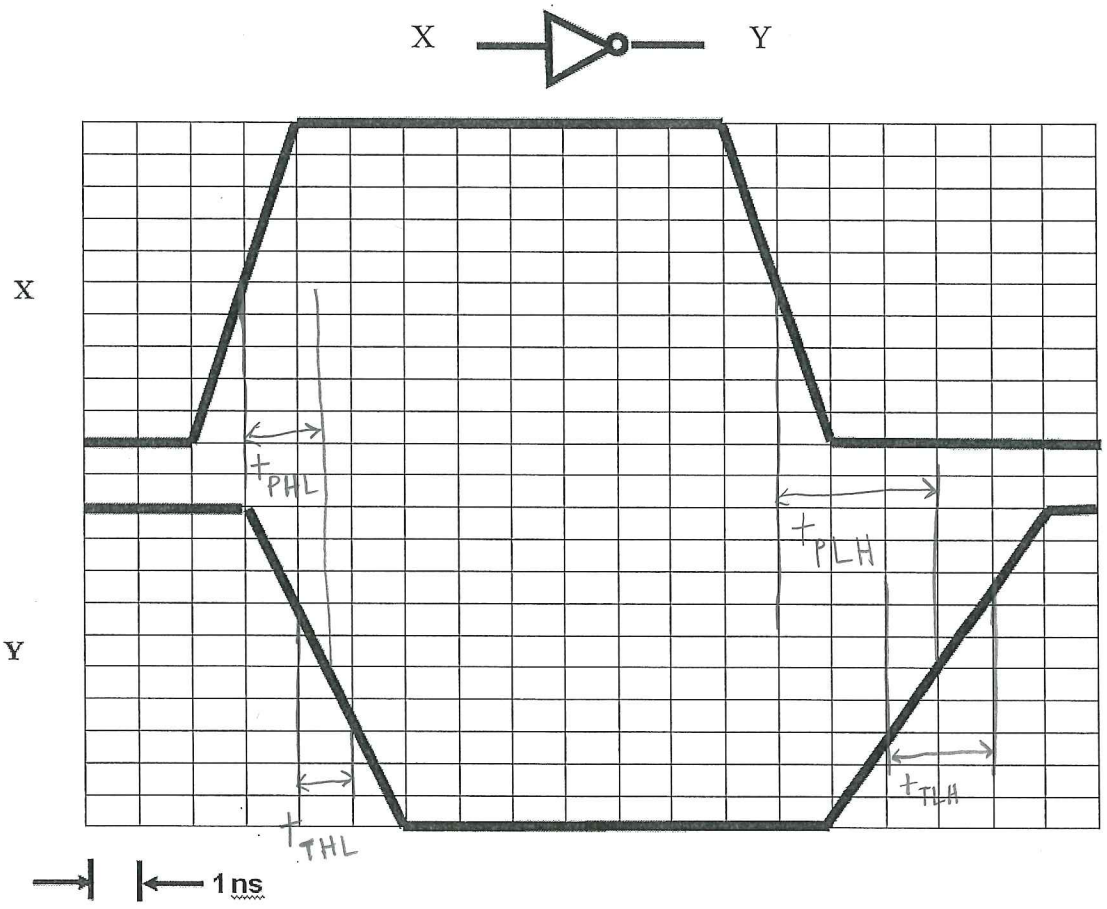
$= 300\Omega$

$P_R = V_{Total} \times I_{OLmax} = 3V(10mA) = 30mW$

Current limiting resistor = 300 Ω **Resistor power dissipation =** 30 mW

In-Class Homework for Module 1 – No. 5
Wednesday, January 29, 2014

The timing diagram below depicts the input and output signals of an inverter. Determine the approximate t_{TLH}, t_{THL}, t_{PLH}, and t_{PHL} of the inverter.



The rise time (t_{TLH}) for the inverter is approximately: 2 ns

The fall time (t_{THL}) for the inverter is approximately: 1 ns

The fall propagation delay (t_{PHL}) for the inverter is approximately: 1.5 ns

The rise propagation delay (t_{PLH}) for the inverter is approximately: 3 ns

Given that a (5-volt) CMOS gate's P-channel output pull-up has an "on" resistance of 100Ω and that its N-channel output pull-down has an "on" resistance of 50Ω:

(a) If the desired I_{OH} and I_{OL} are 5 mA (i.e., -5 mA for I_{OH}, +5 mA for I_{OL}), then the V_{OH} and V_{OL} specifications for this gate will be:

$$\frac{V_{CC}-V_{OH}}{R_P} = I_{OH}$$
$$R_P I_{OH} = V_{CC}-V_{OH}$$
$$R_P I_{OH} - V_{CC} = -V_{OH}$$
$$V_{CC} - R_P I_{OH} = V_{OH}$$
$$5\,V - 100\Omega\,(5mA) = V_{OH}$$

$V_{OH} =$ 4.5V

$$\frac{V_{OL}-V_{GND}}{R_n} = I_{OL}$$
$$R_n I_{OL} = V_{OL}-V_{GND}$$
$$R_n I_{OL} + V_{GND} = V_{OL}$$
$$50\Omega\,(5mA) + 0V = V_{OL}$$
$$0.25V = V_{OL}$$

$V_{OL} =$ 0.25V

(b) If the V_{IHmin} and V_{ILmax} specifications are 3.5 volts and 1.5 volts, respectively, then the DCNM for this gate will be:

$$DCNM = \min(V_{OHmin} - V_{IHmin},\ V_{ILmax} - V_{OLmax})$$
$$= \min(4.5V - 3.5V,\ 1.5V - 0.25V)$$
$$= \min(1.0V,\ 1.25V)$$
$$= 1.0V$$

DCNM = 1.0V

(c) If a gate from this family drives a capacitive load of 100 pF, estimate its rise and fall times.

$$R_p C_L =$$
$$= 100\Omega\,(100pF)$$
$$= 100\Omega \times (100 \times 10^{-12}F)$$
$$= 10\,ns$$

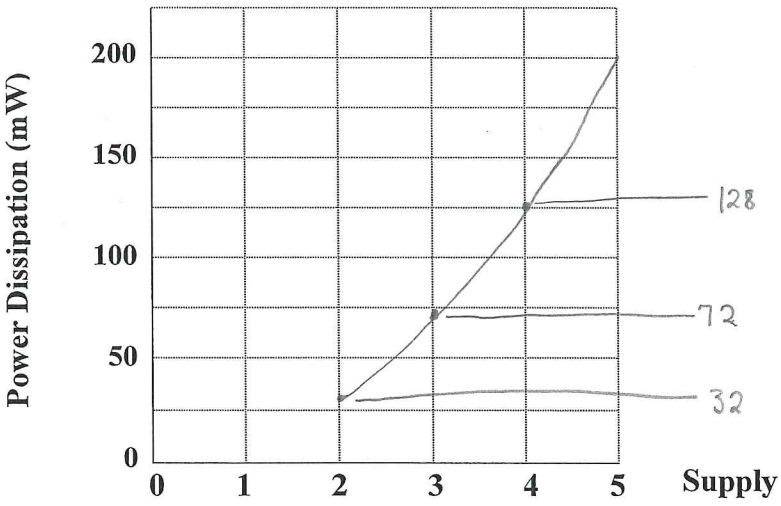
$$R_n C_L =$$
$$= 50\Omega\,(100pF)$$
$$= 50\Omega\,(100 \times 10^{-12}F)$$
$$= 5\,ns$$

Rise time estimate = 10 **ns** **Fall time estimate =** 5 **ns**

In-Class Homework for Module 1 – No. 6
Friday, January 31, 2014

A particular CMOS microcontroller is design to operate over a supply voltage range of 2 V to 5 V and at a maximum clock frequency of 100 MHz (no minimum clock frequency is specified). The maximum power dissipation over this range of supply voltage and clock frequency is specified to be 200 milliwatts.

(a) Plot the relationship between *power dissipation* and *supply voltage* for this microcontroller.



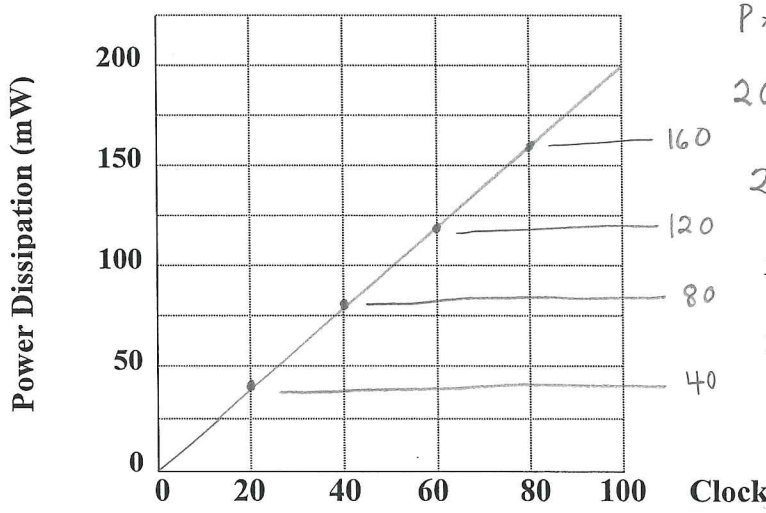
$P \times \left(\frac{\text{Supply Voltage}}{\text{Total Supply Voltage}}\right)^2 =$

$200 \times \left(\frac{2}{5}\right)^2 = 32\,mW$

$200 \times \left(\frac{3}{5}\right)^2 = 72\,mW$

$200 \times \left(\frac{4}{5}\right)^2 = 128\,mW$

(b) Plot the relationship between *power dissipation* and *clock frequency* for this microcontroller.



$P \times \left(\frac{\text{Clock Frequency}}{\text{Max. Clock Frequency}}\right) =$

$200 \times \frac{20}{100} = 40\,mW$

$200 \times \frac{40}{100} = 80\,mW$

$200 \times \frac{60}{100} = 120\,mW$

$200 \times \frac{80}{100} = 160\,mW$

Assume a CMOS microprocessor dissipates *100 milliwatts* of power when operated at a clock frequency of *100 MHz* with a supply voltage of *5 V*. *If the frequency of operation is reduced from 100 MHz to 40 MHz* (and the supply voltage remains 5 V), the power dissipation will be reduced to:

$$P \times \left(\frac{\text{Clock Frequency}}{\text{Max. Clock Frequency}}\right) =$$

$$= 100 \times \frac{40}{100}$$

$$= 40 \text{ mW}$$

Assume a CMOS microprocessor dissipates *100 milliwatts* of power when operated at a clock frequency of *100 MHz* with a supply voltage of *5 V*. *If the supply voltage is reduced from 5 V to 4 V* (and the frequency of operation remains 100 MHz), the power dissipation will be reduced to:

$$P \times \left(\frac{\text{Supply Voltage}}{\text{Total Supply Voltage}}\right)^2 =$$

$$= 100 \times \left(\frac{4}{5}\right)^2$$

$$= 100 \times \frac{16}{25}$$

$$= 64 \text{ mW}$$

Assume a CMOS microprocessor dissipates *100 milliwatts* of power when operated at a clock frequency of *100 MHz* with a supply voltage of *5 V*. *If the supply voltage is reduced from 5 V to 2 V* and *if the frequency of operation is reduced from 100 MHz to 50 MHz*, the power dissipation will be reduced to:

$$P \times \left(\frac{\text{Supply Voltage}}{\text{Total Supply Voltage}}\right)^2 \times \left(\frac{\text{Clock Frequency}}{\text{Max. Clock Frequency}}\right) =$$

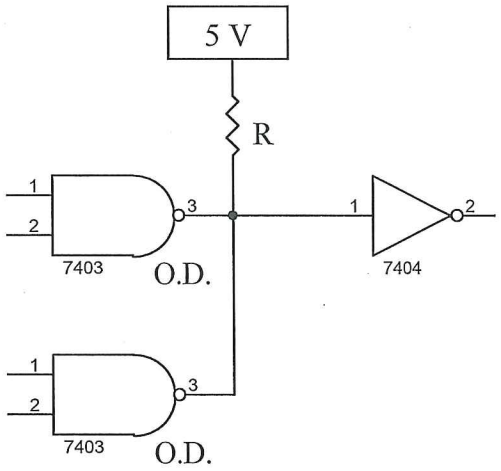
$$= 100 \times \left(\frac{2}{5}\right)^2 \times \frac{50}{100}$$

$$= 100 \times \frac{4}{25} \times \frac{50}{100}$$

$$= 8 \text{ mW}$$

In-Class Homework for Module 1 – No. 7
Monday, February 3, 2014

Given the following circuit:



(a) **For the case of BOTH inputs of BOTH gates driven LOW: If the off-state leakage current of each of the 74x03 open-drain NAND gate outputs is +5 μA, and the I_{IH} required by the 74x04 inverter is +490 μA, determine the *maximum* value of R that will produce a V_{IH} of *at least* 4.5 volts at the 74x04 input.**

Current through R: $I_R = 5\mu A + 5\mu A + 490\mu A$
$= 500\mu A$

Voltage drop across R: $V_R = V_{CC} - V_{IH} = 5V - 4.5V$
$= 0.5V$

$$R = \frac{V_R}{I_R} = \frac{0.5V}{500\mu A} = 1000\,\Omega$$

Maximum R = 1000Ω

(b) **For the case of both inputs of ONE gate driven HIGH and both inputs of the other gate driven LOW: If the I_{OLmax} of the 74x03 is specified to be +10 mA and that the I_{IL} required by the 74x04 inverter is -1 mA, determine the *minimum* value of R the will produce a V_{IL} of *no more than* 0.5 volts at the 74x04 input (assume the same off-state leakage current as Part (a), and round your answer to the nearest Ohm).**

Current through R: $I_R = 10mA - 1mA$
$= 9mA$

Voltage drop across R: $V_{CC} - V_{IL} = 5V - 0.5V$
$= 4.5V$

$$R = \frac{V_R}{I_R} = \frac{4.5V}{9mA} = 500\,\Omega$$

Minimum R = _____

(c) **If you were guest starring on the hit TV series *Power of 10*$_2$ and you were forced to choose one of these two values (i.e., the "Maximum R" or the "Minimum R"), *which* value would you choose, and *why*?**

Which value would you pick (*circle one*): Minimum –or– Maximum

Why?

Minimum (Performance)

Advantage - faster t_{TLH} (rise time)

Disadvantage - maximum power dissipation

Maximum (Power dissipation)

Advantage - minimizes power dissipation

Disadvantage - rise time is considerably longer