Revisited Concept Exercises for Module 2 – No. 1
Monday, February 17, 2014

Given the truth table, below, determine the following:

X	Y	Z	F(X,Y,Z)
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

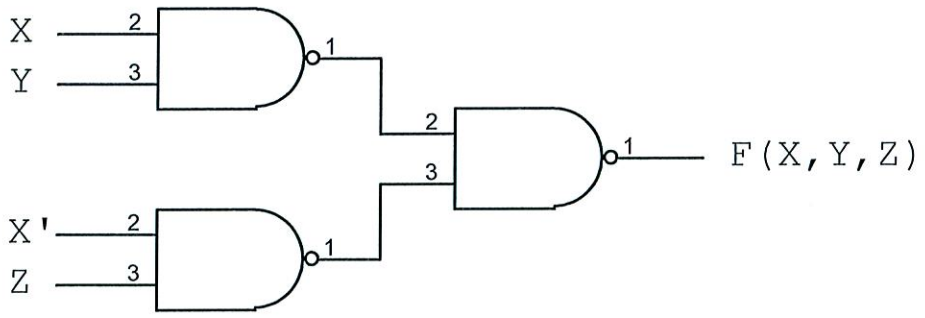
F(X,Y,Z) expressed as:

an *on-set:* _____

an *off-set:* _____

Revisited Concept Exercise for Module 2 – No. 1a
Monday, February 17, 2014

Write out the function, fill out the truth table, and determine both the ON-set and the OFF-set for the function implemented by the following circuit:



F(X,Y,Z) = _____

X	Y	Z	F(X,Y,Z)
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

ON-set = _____

OFF-set = _____

Revisited Concept Exercise for Module 2 – No. 2
Wednesday, February 19, 2014

Compare the cost of minimal two-level NAND and two-level NOR gate implementations of the function, F(W,X,Y,Z), mapped below. Show both the NAND and NOR circuit realizations and calculate the cost of each. Assume both true and complemented variables are available.

NAND realization: **NAND cost =** _____

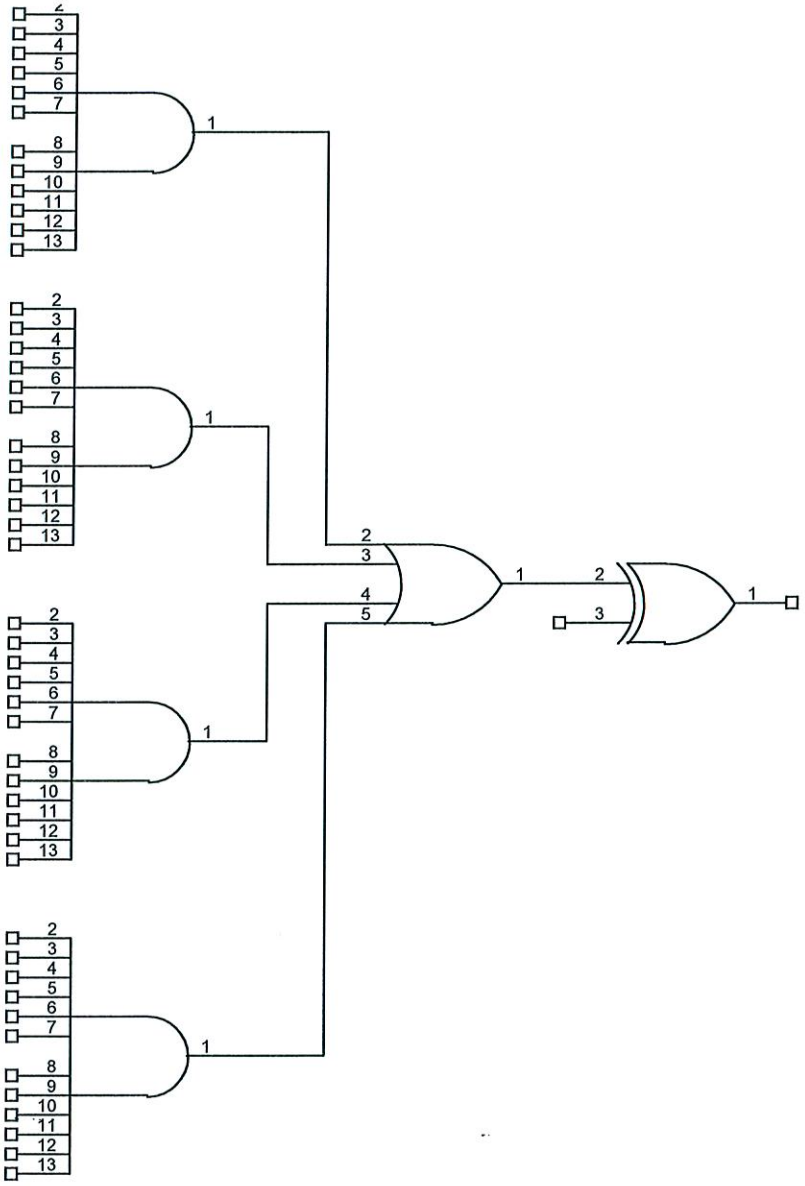
		W′		W	
		0	1	1	0	Z′
Y′		0	0	0	0	
		1	1	0	1	Z
Y		1	1	1	1	Z′
		X′	X		X′	

NOR realization: **NOR cost =** _____

		W′		W	
		0	1	1	0	Z′
Y′		0	0	0	0	
		1	1	0	1	Z
Y		1	1	1	1	Z′
		X′	X		X′	

Revisited Concept Exercise for Module 2 – No. 3
Monday, February 24, 2014

Assume a hypothetical PLD has macrocells of the following configuration:



The maximum number of *product terms* that can be implemented by each macrocell = ____

The maximum number of *literals* that each product term can have = ____

Revisited Concept Exercise for Module 2 – No. 4
Wednesday, February 26, 2014

1. **`A0`, `A1`, `A2`, `A3` defined as the set `ALL`:**

2. **`B0`, `B1`, `B2`, `B3`, `B4` used as a range:**

3. **`GE` used as the tri-state enable for output signals `G0`, `G1`, `G2`, `G3`:**

4. **Write using ABEL syntax: $G(W,X,Y,Z) = (X \oplus Z) \cdot (W \oplus Y)'$**

5. **Write using ABEL syntax: $F(W,X,Y,Z) = W' \cdot Z \cdot (X + Y') + Y \cdot (X' + W + Z)$**

6. **ABEL declaration that specifies input variables `SA`, `SB`, and `SC` are *active low*:**

7. **ABEL declaration that specifies variables `R0`, `R1`, `R2`, and `R3` are *active low* combinational outputs:**

8. **ABEL equation statement specifying that the *tri-state enable* for combinational output signals `R0`, `R1`, `R2`, and `R3` is given by the expression $A \cdot B' \cdot C$:**