In-Class Homework for Module 2 – No. 1
Monday, February 17, 2014

Given the truth table, below, determine the following:

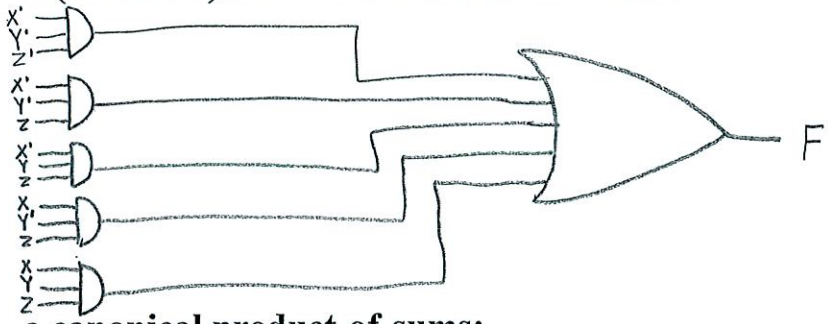
X	Y	Z	F(X,Y,Z)
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

F(X,Y,Z) expressed as:

- a canonical sum-of-products:

$$F(X,Y,Z) = X'\cdot Y'\cdot Z' + X'\cdot Y'\cdot Z + X'\cdot Y\cdot Z + X\cdot Y'\cdot Z' + X\cdot Y\cdot Z$$

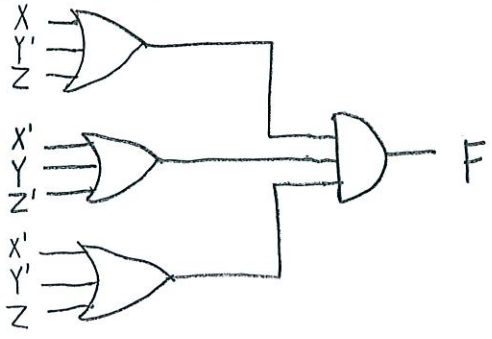
- a (two-level) AND-OR circuit realization:



- a canonical product-of-sums:

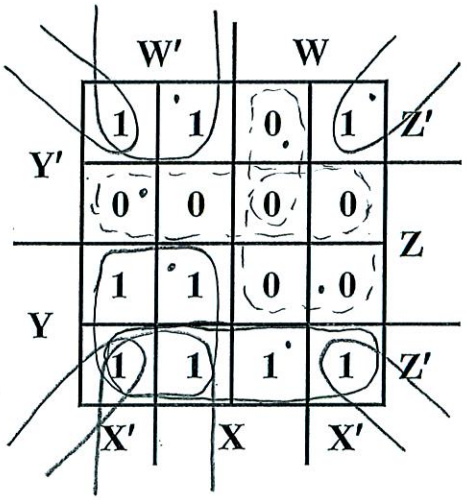
$$F(X,Y,Z) = (X + Y' + Z)\cdot(X' + Y + Z')\cdot(X' + Y' + Z)$$

- a (two-level) OR-AND circuit realization:



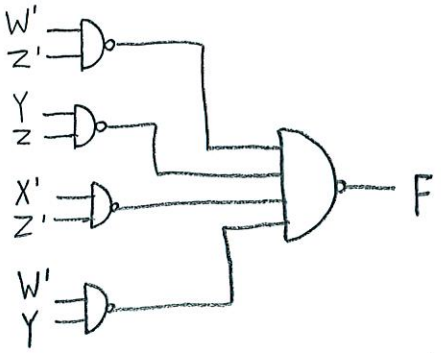
In-Class Homework for Module 2 – No. 1a
Monday, February 17, 2014

1. For the function mapped below:



- Write a minimal sum-of-products expression and draw a NAND-NAND realization:

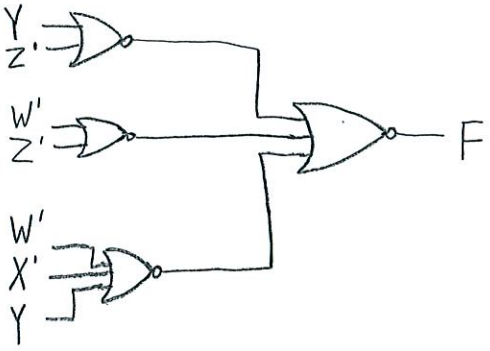
$F = W' \cdot Z' + Y \cdot Z' + X' \cdot Z' + W' \cdot Y$



- Write a minimal product-of-sums expression and draw a NOR-NOR realization:

$F' = Y' \cdot Z + W \cdot Z + W \cdot X \cdot Y'$

$F = (Y + Z') \cdot (W' + Z') \cdot (W' + X' + Y)$



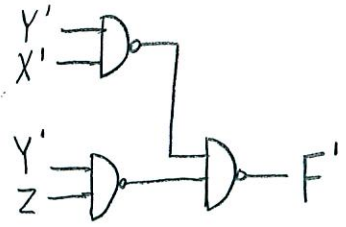
2. Express the *complement* of the following function as an ON SET and draw a NAND-NAND realization:

$$F(X,Y,Z) = Y + X \cdot Z'$$

$$F'(X,Y,Z) = Y' \cdot (X' + Z)$$

$$= Y' \cdot X' + Y' \cdot Z$$

	X'		X	
Z'	0 1	2 0	6 0	4 0
Z	1 1	3 0	7 0	5 0
	Y'	Y		Y'



$$\sum_{X,Y,Z}(0,1,5)$$

---

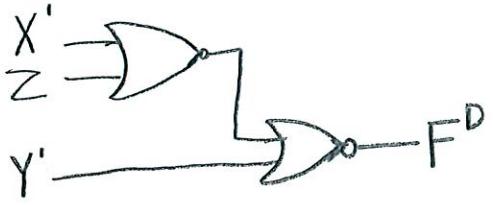
3. Express the *dual* of the following function as an OFF SET and draw a NOR-NOR realization:

$$F(X,Y,Z) = Y + X' \cdot Z$$

$$F^D(X,Y,Z) = Y \cdot (X' + Z)$$

$$= Y \cdot X' + Y \cdot Z$$

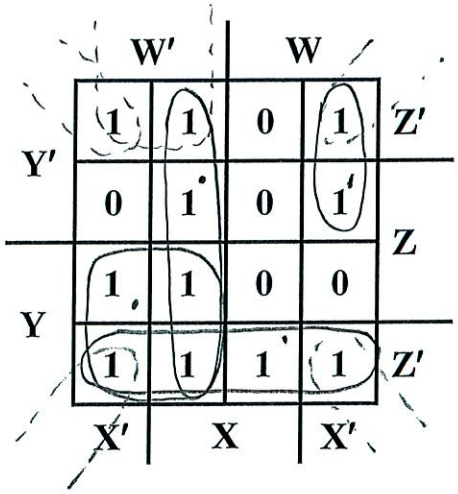
	X'		X	
Z'	0 0	2 1	6 0	4 0
Z	1 0	3 1	7 1	5 0
	Y'	Y		Y'



$$\Pi_{X,Y,Z}(0,1,4,5,6)$$

In-Class Homework for Module 2 – No. 1b
Monday, February 17, 2014

In determining a minimal sum-of-products expression for the function mapped below, indicate whether the following statements are true or false:



(T) F The term W′•Y is an essential prime implicant.

T (F) The term X′•Z′ is an essential prime implicant.

T (F) The term W′•Z′ is an essential prime implicant.

(T) F The term W′•X is an essential prime implicant.

(T) F The term Y•Z′ is an essential prime implicant.

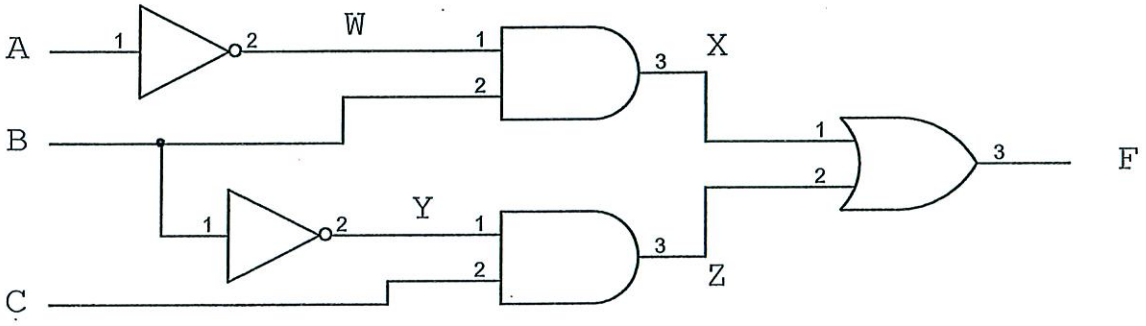
(T) F The term W•X′•Y′ is an essential prime implicant.

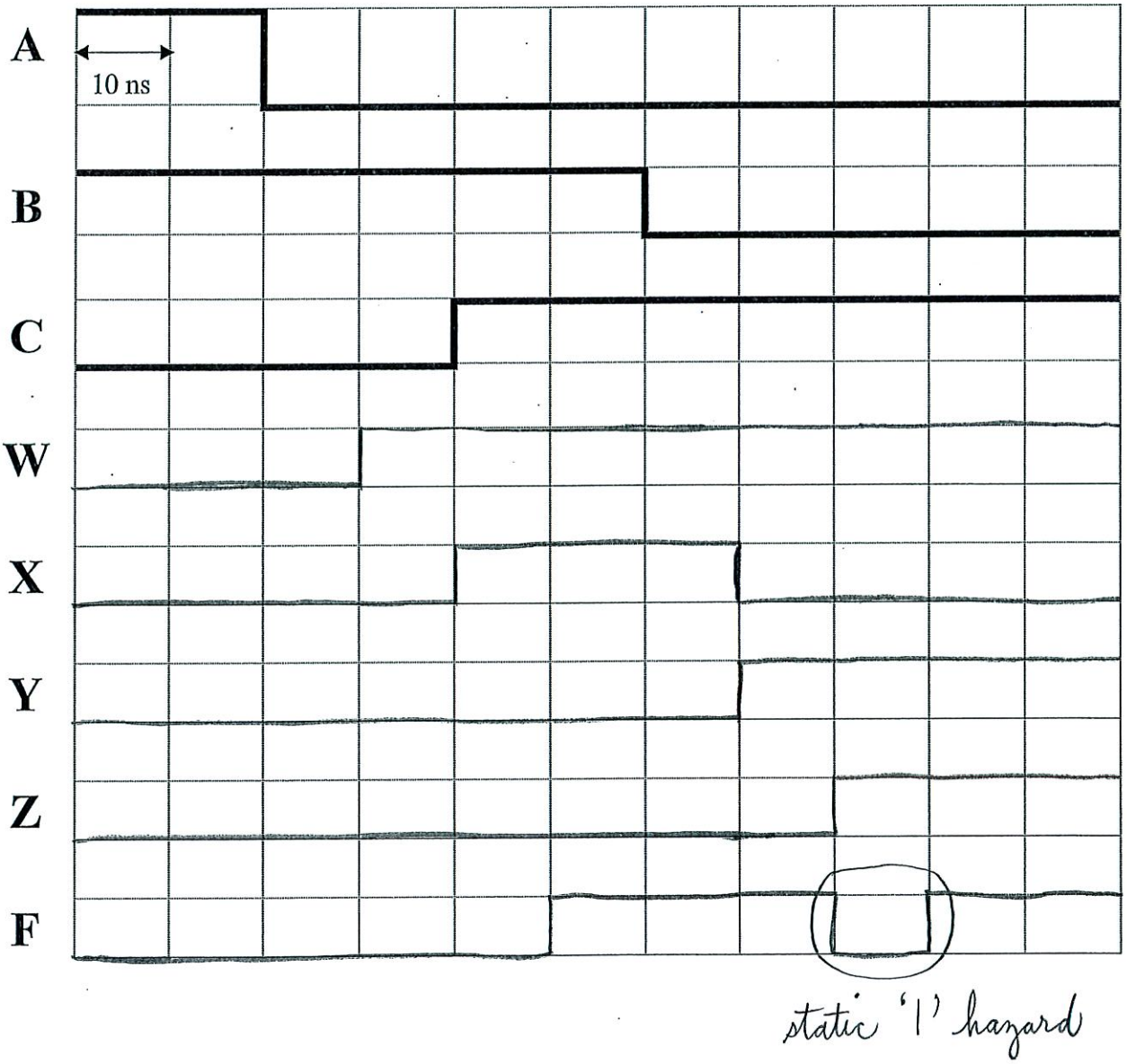
Write a minimum sum-of-products expression for this function:

F(W,X,Y,Z) = $W \cdot X' \cdot Y' + Y \cdot Z' + W' \cdot Y + W' \cdot X + X' \cdot Z'$ or $W' \cdot Z'$

In-Class Homework for Module 2 – No. 2
Wednesday, February 19, 2014

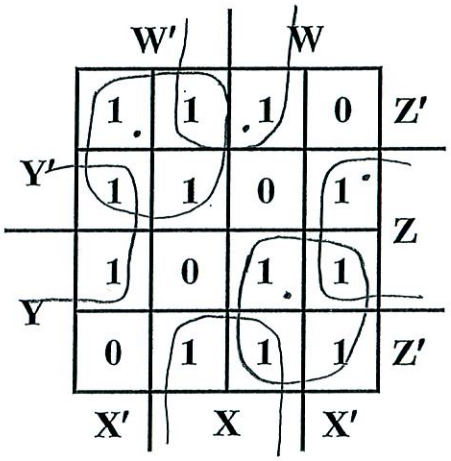
1. **Sketch the response of the circuit, below, to the input signals provided. Assume the input signals (A, B, C) have been in the initial states shown prior to the beginning of the chart, and that each gate has a t_{PLH} and t_{PHL} of 10 ns. *Identify the hazard* (by name) if one occurs in the output (F).**



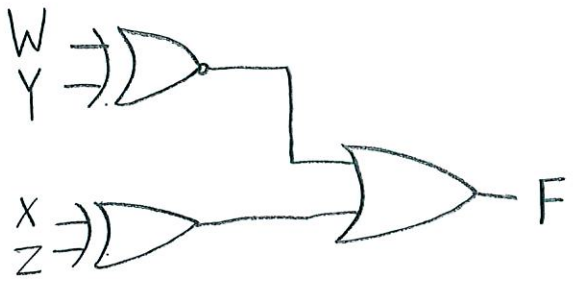


static '1' hazard

2. Determine if the function mapped below can be *simplified* in terms of XOR or XNOR operators.



$$F = W' \cdot Y' + W \cdot Y + X' \cdot Z + X \cdot Z'$$
$$= (W \oplus Y)' + X \oplus Z$$



In-Class Homework for Module 2 – No. 3
Monday, February 24, 2014

1. **Write an ABEL file that realizes the following functions in a 22V10 PLD:**
   - **F(A,B,C,D,E) = A′·B·C + A·B′·C′·E + B·C·D′·E′ + A·B·C′·D**
   - **G(A,B,C,D,E) = A′·D·E′ + B′·C′·E′ + A·C·E + B·D·E**

```
MODULE Problem1

TITLE 'Module 3A Problem 1'

DECLARATIONS

a,b,c,d,e pin;

f,g pin istype 'com';

EQUATIONS

f = !a&b&c # a&!b&!c&e # b&c&!d&!e
    # a&b&!c&d;

g = !a&d&!e # !b&!c&!e # a&c&e # b&d&e;

END
```

2. Write an ABEL file that realizes the following truth table in a 22V10 PLD:

X	Y	Z	F(X,Y,Z)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

```
MODULE Problem2

TITLE 'Module 3A Problem 2'

DECLARATIONS

x,y,z pin;

f pin istype 'com';

truth_table ([x,y,z]->[f])
             [0,0,0]->[0];
             [0,0,1]->[0];
             [0,1,0]->[0];
             [0,1,1]->[1];
             [1,0,0]->[0];
             [1,0,1]->[1];
             [1,1,0]->[1];
             [1,1,1]->[1];
END
```

In-Class Homework for Module 2 – No. 4
Wednesday, February 26, 2014

Demonstrate that you can implement *any* arbitrary 3-variable Boolean function using *just* a 3:8 decoder with active low outputs (specifically, a 74x138) and a *single* 4-input NAND gate (plus some resistors and an LED).

HINT: The LED may be connected in either a sourcing or a sinking configuration.

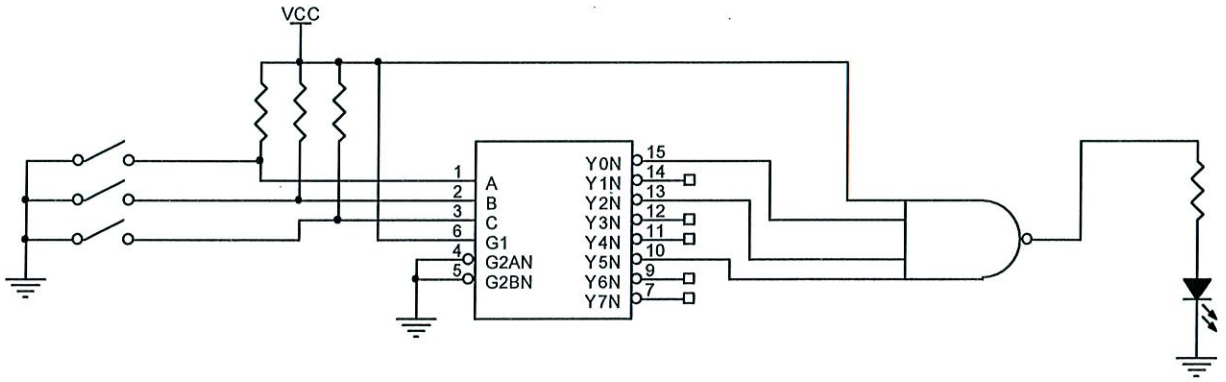
(a) **Implement the function $F(C,B,A) = C'A' + C \cdot B' \cdot A$**

Derivation:

	C′		C		
A′	1	1	0	0	$\Sigma_{C,B,A}$ (0,2,5)
A	0	0	0	1	
	B′	B		B′	

Use 1's (since fewer of them)

Yields F → source current to LED



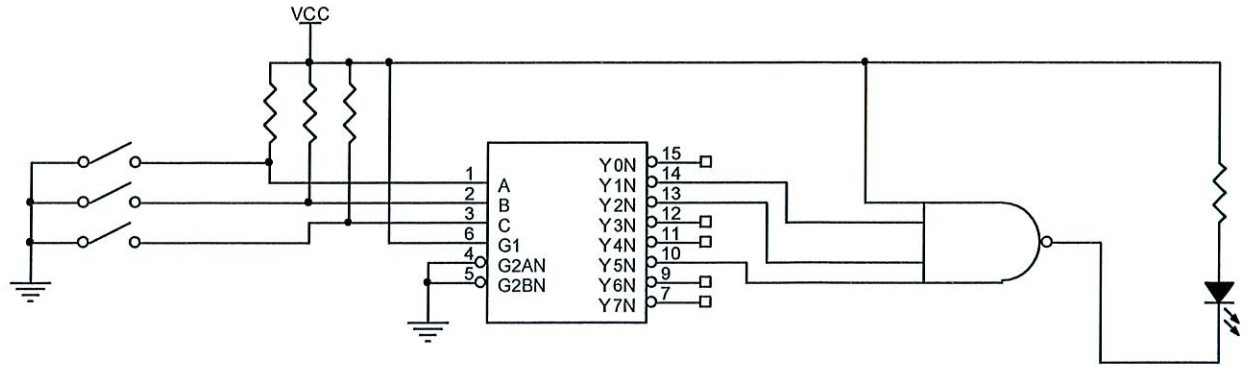
(b) **Implement the function $F(C,B,A) = C' \cdot B' \cdot A' + B \cdot A + C \cdot A'$**

Derivation:

	C′		C		
A′	1	0	1	1	$\Pi_{C,B,A}$ (1,2,5)
A	0	1	1	0	
	B′	B		B′	

Use 0's (since fewer of them)

Yields F′ → sink current through LED



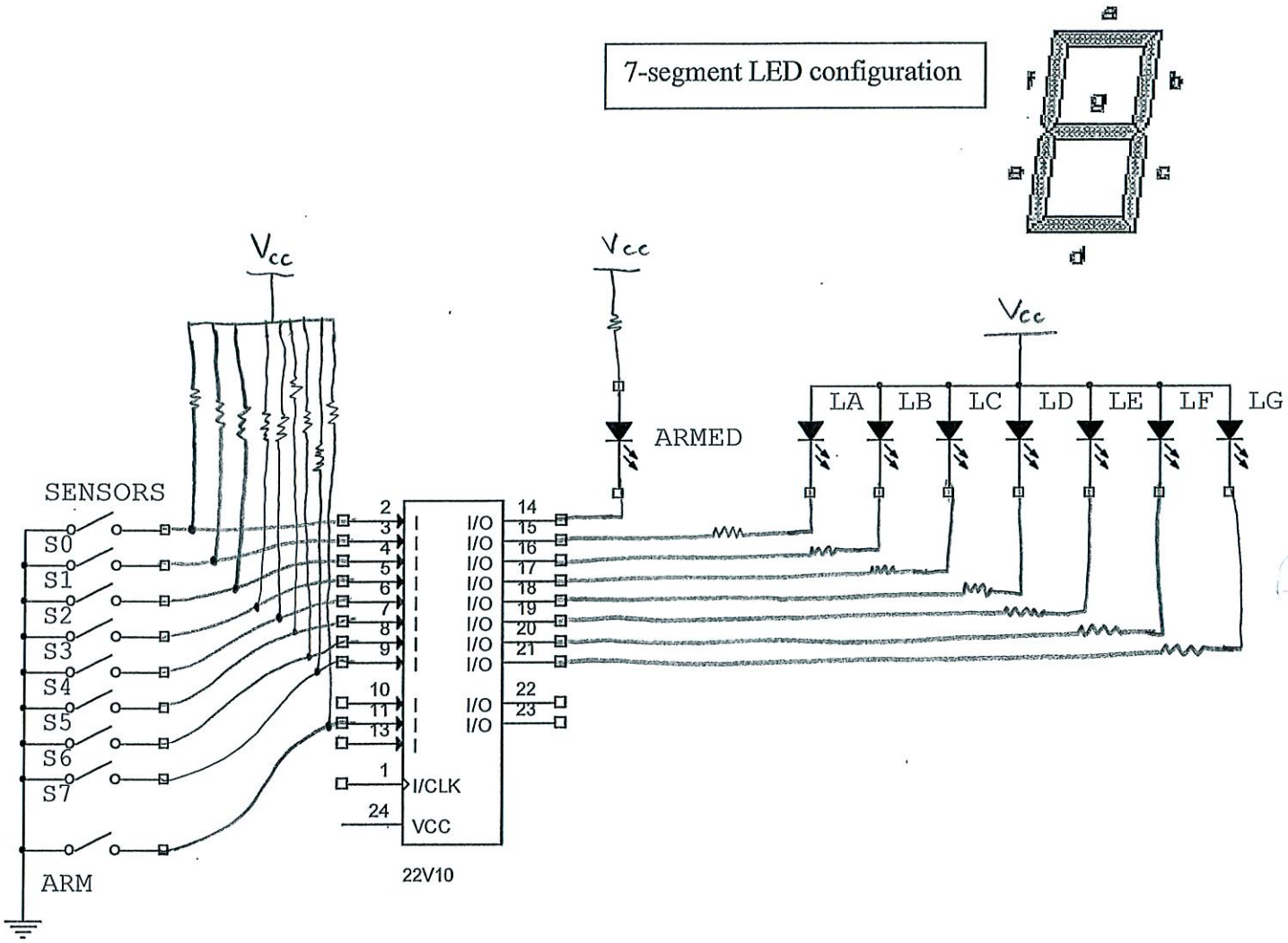
In-Class Homework for Module 2 – No. 4a
Wednesday, February 26, 2014

Complete the ABEL file, below, that implements a "dorm-room alarm" system using a 22V10 PLD. Your alarm should accommodate eight sensor inputs, labeled **S0** through **S7**, plus an **ARM** input that can be used to arm the alarm. If any sensors are asserted while the alarm is armed, the number of the highest sensor asserted will be displayed on a 7-segment common-anode LED. Note that there are a total of nine (active high) inputs and eight (active low) outputs. In summary, the alarm should function as follows:

- If the **ARM** input is negated, the **ARMED** output indicator should be *off* and the 7-segment LED should be *blank.*
- If the **ARM** input is asserted but all the sensors are negated, the **ARMED** output indicator should be *on* and the 7-segment LED should be *blank.*
- If the **ARM** input is asserted, the **ARMED** output indicator should be on and the *highest numbered input* asserted should be displayed on a common anode 7-segment LED.

```
MODULE dormalm

TITLE 'Prioritized Dorm Alarm with 7-segment Display'

DECLARATIONS
S0..S7 pin 2..9;     " sensor inputs
ARM pin 11;          " ARM (enable) input
LA,!LB,!LC,!LD,!LE,!LF,!LG pin 15..21 istype 'com'; " 7-segment display outputs
!ARMED pin 14 istype 'com';      " ARMED output
X = .X.;             " short hand for don't care

TRUTH_TABLE
 ([ARM, S7, S6, S5, S4, S3, S2, S1, S0] -> [ARMED, LA, LB, LC, LD, LE, LF, LG])
  [ 0, X, X, X, X, X, X, X, X] -> [ 0,  0, 0, 0, 0, 0, 0, 0]; "off
  [ 1, 0, 0, 0, 0, 0, 0, 0, 0] -> [ 1,  0, 0, 0, 0, 0, 0, 0]; "off
  [ 1, 0, 0, 0, 0, 0, 0, 0, 1] -> [ 1,  1, 1, 1, 1, 1, 1, 0]; "0
  [ 1, 0, 0, 0, 0, 0, 0, 1, X] -> [ 1,  0, 1, 1, 0, 0, 0, 0]; "1
  [ 1, 0, 0, 0, 0, 0, 1, X, X] -> [ 1,  1, 1, 0, 1, 1, 0, 1]; "2
  [ 1, 0, 0, 0, 0, 1, X, X, X] -> [ 1,  1, 1, 1, 1, 0, 0, 1]; "3
  [ 1, 0, 0, 0, 1, X, X, X, X] -> [ 1,  0, 1, 1, 0, 0, 1, 1]; "4
  [ 1, 0, 0, 1, X, X, X, X, X] -> [ 1,  1, 0, 1, 1, 0, 1, 1]; "5
  [ 1, 0, 1, X, X, X, X, X, X] -> [ 1,  1, 0, 1, 1, 1, 1, 1]; "6
  [ 1, 1, X, X, X, X, X, X, X] -> [ 1,  1, 1, 0, 0, 0, 0, 0]; "7

END
```

Show a complete schematic for your dorm alarm, including the input switches and LED outputs. Use the 22V10 pin numbering declared in the ABEL file you completed on the previous page. Assume all LEDs have a forward voltage of 1.5 V, that V_{OL} of the PLD outputs is 0.5 V, and that 20 mA of current is to flow through each LED. Add any parts you deem necessary and **indicate their value.**

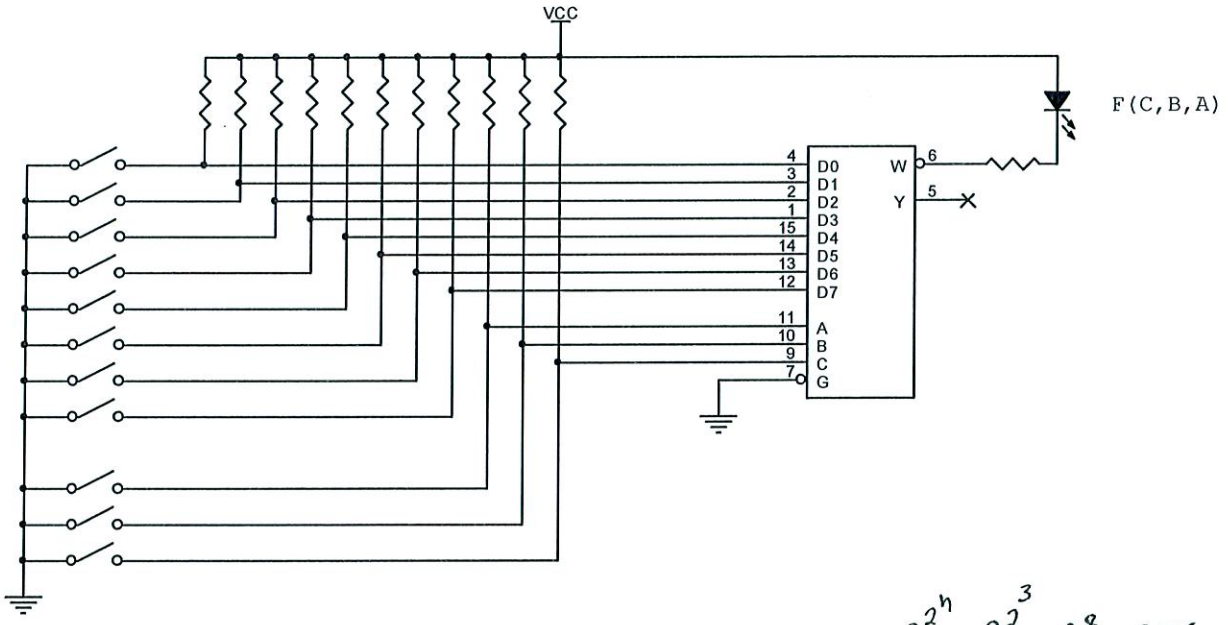


All LED current limiting resistors are = (5-0.5-1.5)/0.020 = 3.0/0.02 = 150Ω

Switch input port pull-up resistors should be 10kΩ (or something in that range).

In-Class Homework for Module 2 – No. 5
Monday, March 3, 2014

Show how you can implement *any* arbitrary 3-variable Boolean function using only an 8:1 multiplexer (specifically, a 74x151), an LED, some resistors, and some DIP switches (note that a "closed" switch should be interpreted as a logic "0", while an "open" switch should be interpreted as a logic "1").



How many *different functions* of three variables are there? **256** $2^{2^n} = 2^{2^3} = 2^8 = 256$

To implement the function **F(C,B,A) = C′·A′ + C·(A⊕B)′** on the circuit, above, determine which "data" switches should be **closed**.

Circle the input switches that should be **closed**: D0 (D1) D2 (D3) D4 (D5) (D6) D7

Show your derivation in the space below:

Derivation:

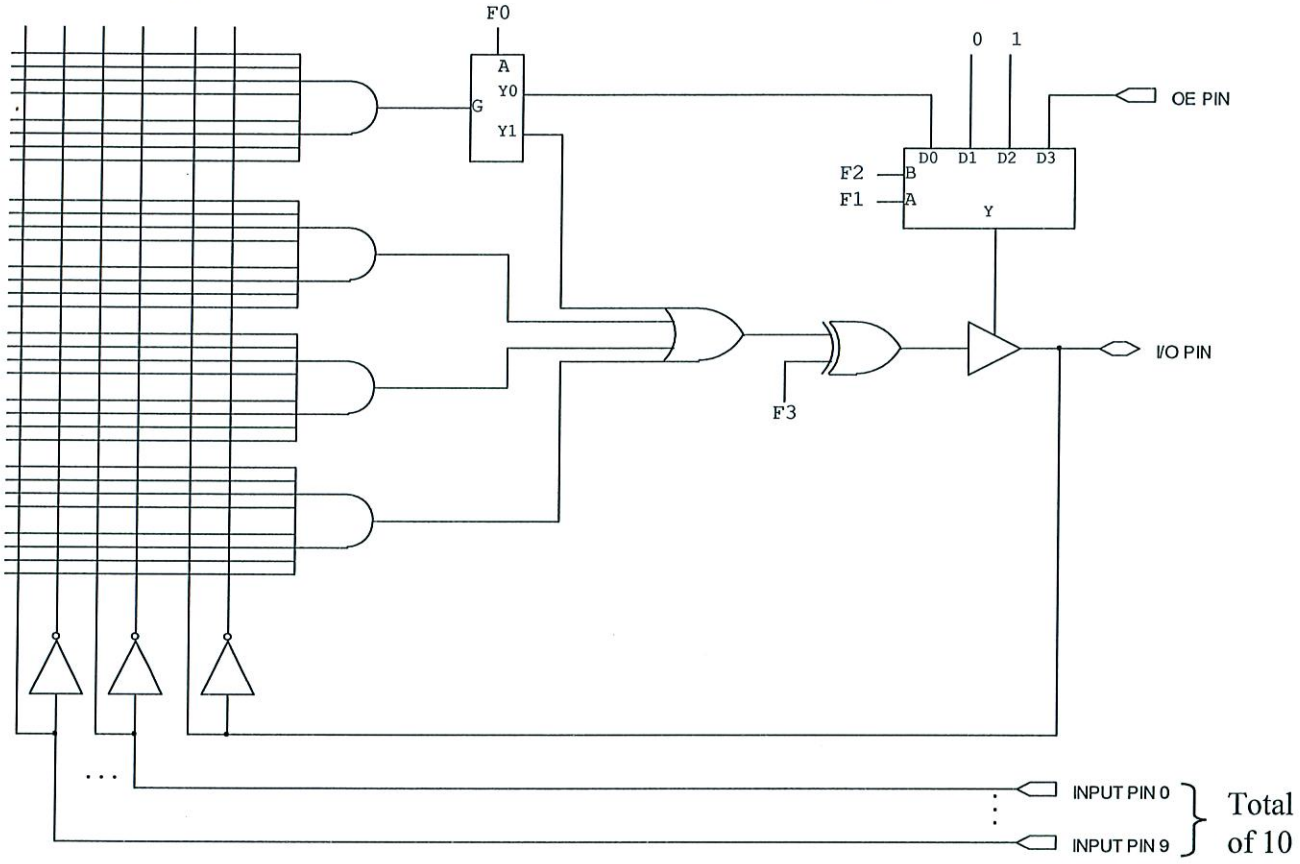
F(C,B,A) = C′·A′ + C·(A⊕B)′
= C′·A′ + C·(B′·A′ + B·A)
= C′·A′ + C·B′·A′ + C·B·A

$\Pi_{C,B,A}$ (1,3,5,6)

	C′		C	
A′	1	1	0	1
A	0	0	1	0
	B′	B		B′

In-Class Homework for Module 2 - No. 5a
Monday, March 3, 2014

Assume a hypothetical PLD has macrocells of the following configuration:



- The maximum number of *product terms* that can be implemented by each macrocell when F0 = 0 is: 3
- The purpose of the *XOR gate* is to: select 0's or 1's of function and/or control pin assertion level
- The purpose of the *demultiplexer* is to: route one of the product terms to tri-state enable or OR gate
- The purpose of the *multiplexer* is to: select the source of the tri-state output enable
- The value to which F1 and F2 should be set to allow the I/O pin to be used as an *input* pin: F2 = 0 F1 = 1
- The value to which F3 should be set to realize the ON SET of a function with an *active low* output: 1
- If F1 = 0 and F2 =0, then F0 must be set to: 0 Reason why: to route output of an AND gate to the tri-state enable