Lecture Summary – Module 1

Switching Algebra and CMOS Logic Gates

Learning Outcome: ***an ability to analyze and design CMOS logic gates***

Learning Objectives:

1-1. convert numbers from one base (radix) to another: 2, 10, 16
1-2. define a binary variable
1-3. identify the theorems and postulates of switching algebra
1-4. describe the principle of duality
1-5. describe how to form a complement function
1-6. prove the equivalence of two Boolean expressions using perfect induction
1-7. describe the function and utility of basic electronic components (resistors, capacitors, diodes, MOSFETs)
1-8. define the switching threshold of a logic gate and identify the voltage ranges typically associated with a "logic high" and a "logic low"
1-9. define assertion level and describe the difference between a positive logic convention and a negative logic convention
1-10. describe the operation of basic logic gates (NOT, NAND, NOR) constructed using N- and P-channel MOSFETs and draw their circuit diagrams
1-11. define "fighting" among gate outputs wired together and describe its consequence
1-12. define logic gate fan-in and describe the basis for its practical limit
1-13. identify key information contained in a logic device data sheet
1-14. calculate the DC noise immunity margin of a logic circuit and describe the consequence of an insufficient margin
1-15. describe the consequences of a "non-ideal" voltage applied to a logic gate input
1-16. describe how unused ("spare") CMOS inputs should be terminated
1-17. describe the relationship between logic gate output voltage swing and current sourcing/sinking capability
1-18. describe the difference between "DC loads" and "CMOS loads"
1-19. calculate V_{OL} and V_{OH} of a logic gate based on the "on" resistance of the active device and the amount of current sourced/sunk by the gate output
1-20. calculate logic gate fan-out and identify a practical lower limit
1-21. calculate the value of current limiting resistor needed for driving an LED
1-22. describe the deleterious effects associated with loading a gate output beyond its rated specifications
1-23. define propagation delay and list the factors that contribute to it
1-24. define transition time and list the factors that contribute to it
1-25. estimate the transition time of a CMOS gate output based on the "on" resistance of the active device and the capacitive load
1-26. describe ways in which load capacitance can be minimized
1-27. identify sources of dynamic power dissipation
1-28. plot power dissipation of CMOS logic circuits as a function of operating frequency
1-29. plot power dissipation of CMOS logic circuits as a function of power supply voltage
1-30. describe the function and utility of decoupling capacitors
1-31. define hysteresis and describe the operation of Schmitt-trigger inputs
1-32. describe the operation and utility of a transmission gate
1-33. define high-impedance state and describe the operation of a tri-state buffer
1-34. define open drain as it applies to a CMOS logic gate output and calculate the value of pull-up resistor needed
1-35. describe how to create "wired logic" functions using open drain logic gates
1-36. calculate the value of pull-up resistor needed for an open drain logic gate

Lecture Summary – Module 1-A

Number Systems

Reference: *Digital Design Principles and Practices* (4th Ed.), pp. 25-34

- **overview**
  - **d_n – digits of base R number**
  - **c_n – converted corresponding digits in base 10**
  - **dealing with *unsigned* numbers only at this point → leading zeroes don't matter**
  - **table of correspondence**

N_2	N_3	N_4	N_5	N_6	N_7	N_8	N_9	N_{10}	N_{16}
0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1
10	2	2	2	2	2	2	2	2	2
11	10	3	3	3	3	3	3	3	3
100	11	10	4	4	4	4	4	4	4
101	12	11	10	5	5	5	5	5	5
110	20	12	11	10	6	6	6	6	6
111	21	13	12	11	10	7	7	7	7
1000	22	20	13	12	11	10	8	8	8
1001	100	21	14	13	12	11	10	9	9
1010	101	22	20	14	13	12	11	10	A
1011	102	23	21	15	14	13	12	11	B
1100	110	30	22	20	15	14	13	12	C
1101	111	31	23	21	16	15	14	13	D
1110	112	32	24	22	20	16	15	14	E
1111	120	33	30	23	21	17	16	15	F
10000	121	100	31	24	22	20	17	16	10

- **integer conversion: base R to base 10**
  - **method: iterative multiply and add**
  - **based on nested expression of a number**

$$(d_3d_2d_1d_0)_R = (N)_{10}$$
$$= c_3xR^3 + c_2xR^2 + c_1xR^1 + c_0xR^0$$
$$= (((c_3 \times R + c_2) \times R + c_1) \times R + c_0)$$

Example: Convert $(4352)_8$ to base 10

$4 \times 8 + 3 = 35$

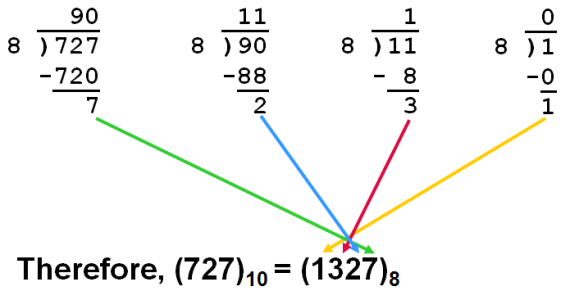
$35 \times 8 + 5 = 285$

$285 \times 8 + 2 = 2282$

Therefore, $(4352)_8 = (2282)_{10}$

- **integer conversion: base 10 to base R**
  - **method: iterative division**
  - **remainders become digits of converted number**
  - **quotient of zero indicates conversion is complete**

Example: Convert $(727)_{10}$ to base 8



Therefore, $(727)_{10} = (1327)_8$

- **short cut for conversion among powers of 2 (from base "A" to base "B")**
  - **method: size $\log_2 R$ groupings**
  - **write an n-digit binary number for each base A digit in the original number, where $n = \log_2 A$**
  - **starting at the least significant position, form m-digit groups, where $m = \log_2 B$**

Example: Convert $(136)_8$ to base 2 and base 16

```
  1       3       6
001     011     110
  0101    1110
  5       E
```

Therefore, $(136)_8 = (\ 1011110\ )_2 = (\ 5E\ )_{16}$

Exercise: Convert $(110101)_2$ to bases 8 and 16

```
    6     5
  110   101
  110101
 0011  0101
    3     5
```

Therefore, $(110101)_2 = (\ 65\ )_8 = (\ 35\ )_{16}$