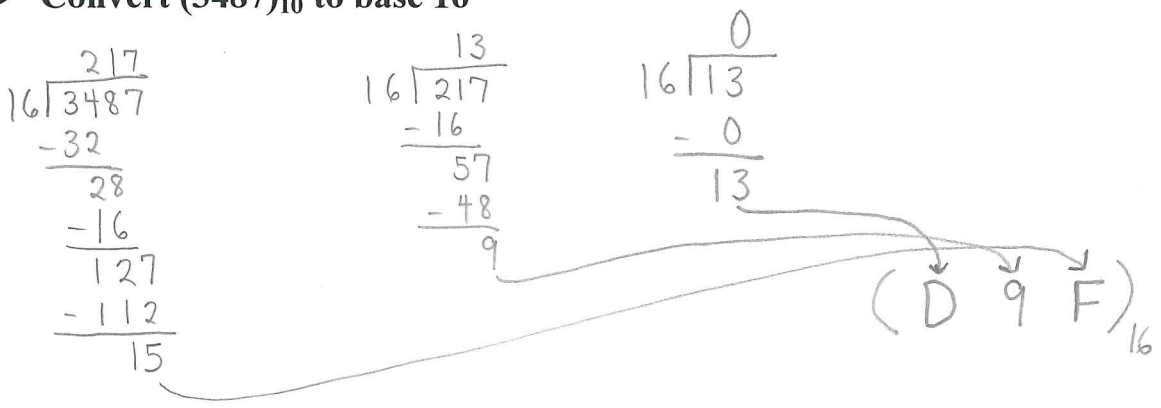
Revisited Concept Exercise for Module 1 – No. 1
Wednesday, January 15, 2014

- **Convert $(1101101)_2$ to base 10**

1 * 2 + 1 = 3
3 * 2 + 0 = 6
6 * 2 + 1 = 13
13 * 2 + 1 = 27
27 * 2 + 0 = 54
54 * 2 + 1 = 109

- **Convert $(3487)_{10}$ to base 16**



- **Convert $(C29E)_{16}$ to base 2**

$(1100\ 0010\ 1001\ 1110)_2$

- **Convert $(1101101)_2$ to base 16**

0110 1101
(6 D)16

Revisited Concepts Exercise for Module 1 – No. 2a
Friday, January 17, 2014

MATCHING – Write the letter of the example (on the right) corresponding to the named axiom or theorem:

I.	**Involution**	**A.**	$(X \cdot Y) \cdot Z = X \cdot (Y \cdot Z)$
D.	**Idempotency**	**B.**	$X+Y = Y+X$
J.	**Identity**	**C.**	$X \cdot Y + X \cdot Y' = X$
F.	**Null Element**	**D.**	$X \cdot X \cdot X = X$
G.	**Complement**	**E.**	$X+(Y \cdot Z) = (X+Y) \cdot (X+Z)$
A.	**Associativity**	**F.**	$X + 1 = 1$
B.	**Commutivity**	**G.**	$X \cdot X' = 0$
E.	**Distributivity**	**H.**	$(X+Y)' = X' \cdot Y'$
C.	**Combining**	**I.**	$(X')' = X$
H.	**DeMorgan's Law**	**J.**	$X + 0 = X$
K.	**Consensus**	**K.**	$X \cdot Y + X' \cdot Z + Y \cdot Z = X \cdot Y + X' \cdot Z$

Revisited Concepts Exercise for Module 1 – No. 2b
Friday, January 17, 2014

MATCHING – Write the letter of the description (on the right) corresponding to the concept or device:

D.	**Capacitor**	**A.**	**Difference in electrical potential**
H.	**Computer**	**B.**	**The flow of charge in a conductor between two points having a difference in potential**
B.	**Current**	**C.**	**Amount of energy**
E.	**Forward Voltage**	**D.**	**A device that stores an electric charge**
F.	**Integrated Circuit (IC or "Chip")**	**E.**	**The voltage drop across a Light Emitting Diode when it is forward biased**
J.	**Microcontroller**	**F.**	**A collection of logic gates and/or other electronic circuits fabricated on a single silicon chip**
I.	**Microprocessor**	**G.**	**An integrated circuit onto which a generic logic circuit can be programmed**
C.	**Power**	**H.**	**A digital device that sequentially executes a stored program**
G.	**Programmable Logic Device (PLD)**	**I.**	**A single-chip embodiment of the major functional blocks of a computer**
A.	**Voltage**	**J.**	**A complete computer on a chip, including integrated peripherals**
M.	**CMOS**	**K.**	**Fiberglass reinforced epoxy substrate with etched copper circuitry (typically in multiple layers) used to create virtually all electronic devices**
L.	**Discrete Logic**	**L.**	**A circuit constructed using small-scale Integrated (SSI) and medium-scale integrated (MSI) logic devices (NAND gates, decoders, Multiplexers, etc.)**
K.	**Printed Circuit Board (PCB)**	**M.**	**A silicon chip fabrication technology based on Use of complementary pairs of NMOS and PMOS field effect transistors (MOSFETs)**

Revisited Concepts Exercise for Module 1 – No. 3
Wednesday, January 22, 2014

1. Describe the function of a P-channel MOSFET:
   When v_{in} is low, the output is high. When v_{in} is high, the P-channel MOSFET is off.

2. When a MOSFET is off, its drain-to-source impedance is on the order of:

   - On the order of Mega (Ω) (Very High)

3. Describe the function of a combinational circuit:
   In a combinational circuit, the outputs depend only on its current inputs.

4. Fill out the truth table for a **NOT** gate:

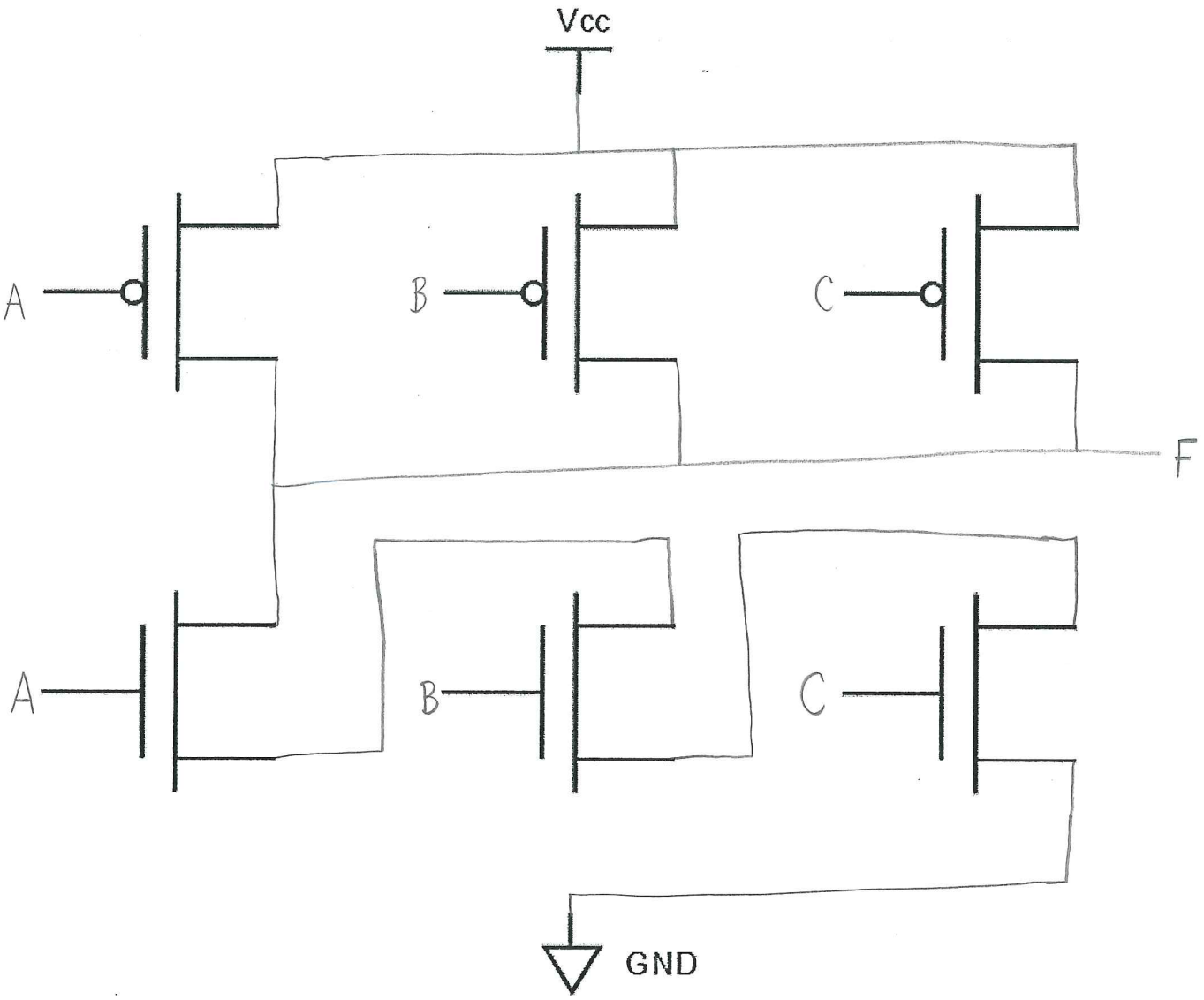
A	(A)′
0	1
1	0

5. If I'm on a deserted island with my DK-1 kit (starring on the *Digital Survivor* show), I can build "anything digital" using only a bucket full of what (single) type of 2-input logic gate? What is the name of the property upon which this premise is based?

   Type of 2-input gate: NAND -or- NOR

   Name of property: Logical completeness

6. Using a total of **three** N-channel MOSFETs and **three** P-channel MOSFETs, draw a circuit schematic for a **three-input NAND** gate. The gate inputs should be labeled A, B, C and the gate output should be labeled F. Be sure to show the power (Vcc) and ground (GND) connections as well.

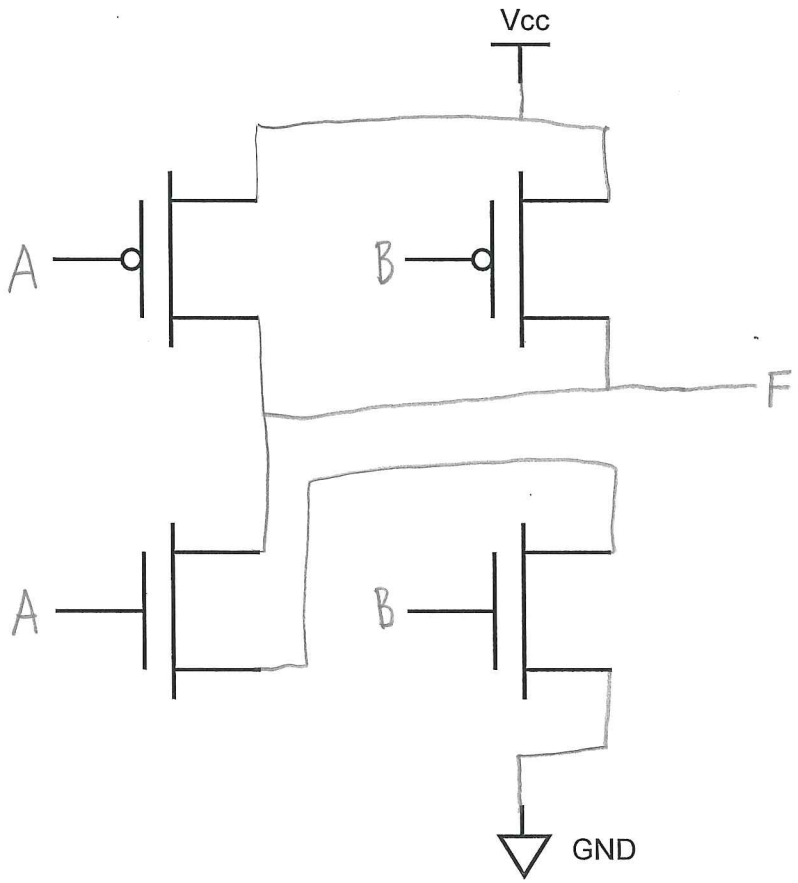


Revisited Concepts Exercise for Module 1 - No. 4
Monday, January 27, 2014

1. Fill out the truth table for a **2-input NAND** gate:

A	B	(A·B)′
0	0	1
0	1	1
1	0	1
1	1	0

2. Draw a MOSFET-level circuit for a **2-input NAND** gate:



Revisited Concepts Exercise for Module 1 – No. 5
Wednesday, January 29, 2014

1. Is it possible to have a negative DCNM? If so, what would it mean?

Yes; There is not enough output voltage to accomodate the input its attempting to drive.

2. What is the minimum DCNM necessary to ensure a functional circuit?

Margins greater than 0.

3. Is it possible to have a negative fan-out? If so, what would it mean?

No; The calculation is incorrect (possibly a sign error).

4. What is the minimum fan-out necessary to ensure a functional circuit?

The minimun fan-out necessary is 1.

5. What is the factor that limits the practical fan-in of a CMOS logic gate?

The additive "on" resistance of series transistors limits the fan-in of CMOS gates to a relatively small number.

Revisited Concepts Exercise for Module 1 – No. 6
Friday, January 31, 2014

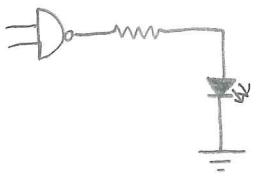
Assume hypothetical logic family has the following D.C. characteristics:

$V_{CC} = 5$ V	$V_{OH} = 3.50$ V	$V_{OL} = 0.50$ V	$V_{IH} = 2.50$ V	$V_{IL} = 1.00$ V
$V_{TH} = (V_{OH} - V_{OL})/2$	$I_{OH} = -5.0$ mA	$I_{OL} = 10$ mA	$I_{IH} = 500$ µA	$I_{IL} = -2.0$ mA

When interfacing an *LED* that has a *forward voltage* of *1.5 V* to this logic family in a *current sourcing* configuration, *maximum brightness* will be achieved (within the rated specifications) using a current limiting resistor of the value along with its power dissipation:

Circuit and calculations:

$$R = \frac{V_{Total}}{I_{OHmin}} = \frac{V_{OH} - V_{LED}}{I_{OHmin}} = \frac{3.50V - 1.5V}{5.0mA} = \frac{2.0V}{5mA} = 400\Omega$$



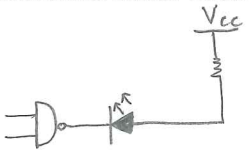
$$P_R = V_{Total} \times I_{OHmin} = 2.0V\,(5.0\,mA) = 10\,mW$$

Current limiting resistor = 400 **Ω** **Resistor power dissipation =** 10 **mW**

When interfacing an *LED* that has a *forward voltage of 1.5 V* to this logic family in a *current sinking* configuration, *maximum brightness* will be achieved (within the rated specifications) using a current limiting resistor of the value along with its power dissipation:

Circuit and calculations:

$$R = \frac{V_{Total}}{I_{OLmax}} = \frac{V_{CC} - V_{OL} - V_{LED}}{I_{OLmax}} = \frac{5V - 0.50V - 1.5V}{10\,mA} = \frac{3.0V}{10mA} = 300\Omega$$



$$P_R = V_{Total} \times I_{OLmax} = 3.0V\,(10\,mA) = 30\,mW$$

Current limiting resistor = 300 **Ω** **Resistor power dissipation =** 30 **mW**

Practice for standardized exam questions — determine the one best response.

1. **When a gate's rated I_{OH} specification is *exceeded*, the following is likely to happen:**
   (A) the V_{OH} of the gate will increase and the t_{TLH} of the gate will decrease
   (B) the V_{OH} of the gate will decrease and the t_{TLH} of the gate will increase
   (C) the V_{OL} of the gate will increase and the t_{THL} of the gate will increase
   (D) the V_{OL} of the gate will decrease and the t_{THL} of the gate will decrease
   (E) none of the above

2. **When a gate's rated I_{OL} specification is *exceeded*, the following is likely to happen:**
   (A) the V_{OH} of the gate will increase and the t_{TLH} of the gate will decrease
   (B) the V_{OH} of the gate will decrease and the t_{TLH} of the gate will increase
   (C) the V_{OL} of the gate will increase and the t_{THL} of the gate will increase
   (D) the V_{OL} of the gate will decrease and the t_{THL} of the gate will decrease
   (E) none of the above

3. **For CMOS gates, V_{IHmin} is typically:**
   (A) 10% of the supply voltage (Vcc)
   (B) 30% of the supply voltage (Vcc)
   (C) 50% of the supply voltage (Vcc)
   (D) 70% of the supply voltage (Vcc)
   (E) 90% of the supply voltage (Vcc)

4. **For CMOS gates, the *switching threshold* is typically:**
   (A) 10% of the supply voltage (Vcc)
   (B) 30% of the supply voltage (Vcc)
   (C) 50% of the supply voltage (Vcc)
   (D) 70% of the supply voltage (Vcc)
   (E) 90% of the supply voltage (Vcc)

5. **The largest source of noise in a digital circuit is from:**
   (A) RF communication devices (e.g., cell phones)
   (B) cosmic rays
   (C) power line disturbances
   (D) the logic gates themselves
   (E) none of the above

6. ***Electromagnetic interference* could cause a "floating" (unconnected) gate input to:**
   (A) change from high-to-low or from low-to-high
   (B) increase the V_{IH} of the gate relative to its specified value
   (C) decrease the V_{IL} of the gate relative to its specified value
   (D) pick up the satellite broadcast of a Purdue basketball victory
   (E) none of the above