Lecture Summary – Module 1

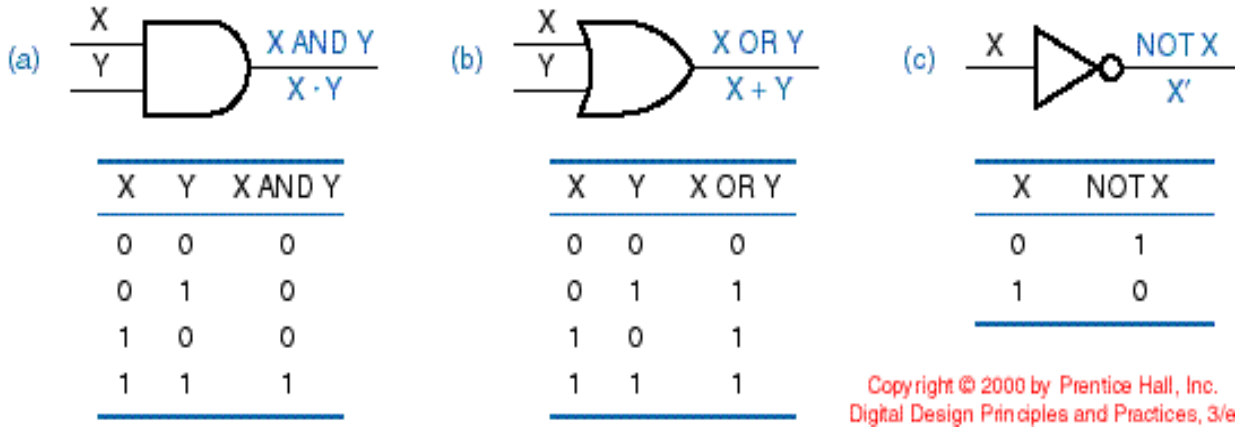
Switching Algebra and CMOS Logic Gates

Learning Outcome: ***an ability to analyze and design CMOS logic gates***

Learning Objectives:

1-1. convert numbers from one base (radix) to another: 2, 10, 16
1-2. define a binary variable
1-3. identify the theorems and postulates of switching algebra
1-4. describe the principle of duality
1-5. describe how to form a complement function
1-6. prove the equivalence of two Boolean expressions using perfect induction
1-7. describe the function and utility of basic electronic components (resistors, capacitors, diodes, MOSFETs)
1-8. define the switching threshold of a logic gate and identify the voltage ranges typically associated with a "logic high" and a "logic low"
1-9. define assertion level and describe the difference between a positive logic convention and a negative logic convention
1-10. describe the operation of basic logic gates (NOT, NAND, NOR) constructed using N- and P-channel MOSFETs and draw their circuit diagrams
1-11. define "fighting" among gate outputs wired together and describe its consequence
1-12. define logic gate fan-in and describe the basis for its practical limit
1-13. identify key information contained in a logic device data sheet
1-14. calculate the DC noise immunity margin of a logic circuit and describe the consequence of an insufficient margin
1-15. describe the consequences of a "non-ideal" voltage applied to a logic gate input
1-16. describe how unused ("spare") CMOS inputs should be terminated
1-17. describe the relationship between logic gate output voltage swing and current sourcing/sinking capability
1-18. describe the difference between "DC loads" and "CMOS loads"
1-19. calculate V_{OL} and V_{OH} of a logic gate based on the "on" resistance of the active device and the amount of current sourced/sunk by the gate output
1-20. calculate logic gate fan-out and identify a practical lower limit
1-21. calculate the value of current limiting resistor needed for driving an LED
1-22. describe the deleterious effects associated with loading a gate output beyond its rated specifications
1-23. define propagation delay and list the factors that contribute to it
1-24. define transition time and list the factors that contribute to it
1-25. estimate the transition time of a CMOS gate output based on the "on" resistance of the active device and the capacitive load
1-26. describe ways in which load capacitance can be minimized
1-27. identify sources of dynamic power dissipation
1-28. plot power dissipation of CMOS logic circuits as a function of operating frequency
1-29. plot power dissipation of CMOS logic circuits as a function of power supply voltage
1-30. describe the function and utility of decoupling capacitors
1-31. define hysteresis and describe the operation of Schmitt-trigger inputs
1-32. describe the operation and utility of a transmission gate
1-33. define high-impedance state and describe the operation of a tri-state buffer
1-34. define open drain as it applies to a CMOS logic gate output and calculate the value of pull-up resistor needed
1-35. describe how to create "wired logic" functions using open drain logic gates
1-36. calculate the value of pull-up resistor needed for an open drain logic gate

- **basic logic gates ("Boolean's Big Three")**
  - **AND – produces a 1 output iff all its inputs are 1**
  - **OR – produces a 1 output if one or more of its inputs are 1**
  - **NOT (inverter) – produces an output value that is the opposite of its input value**

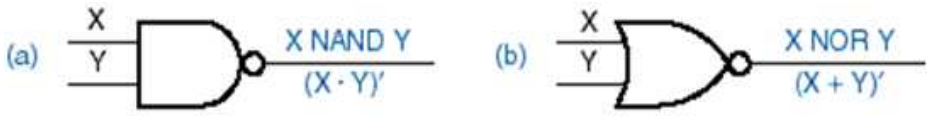


X	Y	X AND Y
0	0	0
0	1	0
1	0	0
1	1	1

X	Y	X OR Y
0	0	0
0	1	1
1	0	1
1	1	1

X	NOT X
0	1
1	0

- **other basic gates (more commonly used)**
  - **NAND ("Not AND") – produces the opposite of an AND gate's output**
  - **NOR ("Not OR") – produces the opposite of an OR gate's output**



X	Y	X NAND Y
0	0	1
0	1	1
1	0	1
1	1	0

X	Y	X NOR Y
0	0	1
0	1	0
1	0	0
1	1	0

NAND and NOR gates are easier to make (require fewer transistors) than AND gates and OR gates

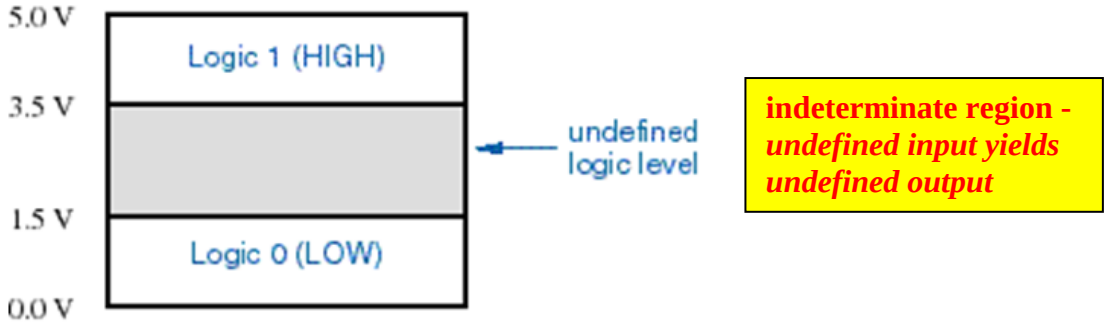
- **logical completeness: "anything digital" can be built using solely AND, OR, and NOT gates -or- solely using NAND gates -or- solely using NOR gates**

Lecture Summary – Module 1-D

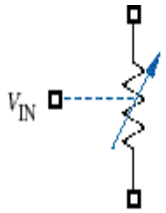
Logic Signals and CMOS Logic Circuits

Reference: *Digital Design Principles and Practices* (4th Ed.), pp. 79-96, 141-148

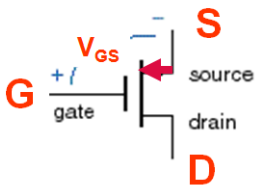
- **overview**
  - **a logic value, 0 or 1, is often referred to as a *binary digit* or *bit***
  - **"LOW" and "HIGH" are often used in place of "0" and "1" to refer to *logic signals***
    - **LOW - a signal in the range of "lower" voltages (e.g., 0 - 1.5 volts for 5V CMOS logic), which is interpreted as a logic 0**
    - **HIGH - a signal in the range of "higher" voltages (e.g., 3.5 - 5.0 volts for 5V CMOS logic), which is interpreted as a logic 1**
  - **the *assignment* of 0 and 1 to LOW and HIGH, respectively, is referred to as a *positive logic convention* (or simply "positive logic")**
    - **a positive logic signal that is *asserted* is in the HIGH state, and is therefore referred to as an "active high" signal**
    - **a positive logic signal that is *negated* is in the LOW state**
  - **the *opposite assignment* (1 to LOW and 0 to HIGH) is referred to as a *negative logic convention* (or "negative logic")**
    - **a negative logic signal that is *asserted* is in the LOW state, and is therefore referred to as an "active low" signal**
    - **a negative logic signal that is *negated* is in the HIGH state**
- **logic families**
  - **complementary metal oxide semiconductor (CMOS) logic is both the most capable and the easiest to understand commercial digital logic technology, and accounts for the vast majority of the worldwide integrated circuit (IC) market**
  - **5-volt CMOS logic levels (other operating voltage ranges proportioned accordingly)**



- **MOS field effect transistor (MOSFET)**
  - **modeled as a 3-terminal device that acts like a voltage-controlled resistance**

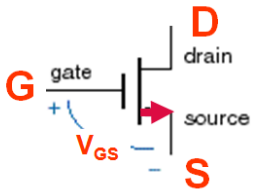


  - **in digital logic applications, MOSFETs are operated so that their resistance is either *very high* (transistor is "off") or *very low* (transistor is "on")**
  - **P-channel MOS (PMOS)**



Voltage-controlled resistance:
decrease V_{GS} → decrease R_{DS}
(current flows from S terminal to D)
Note: normally, $V_{GS} \leq 0$

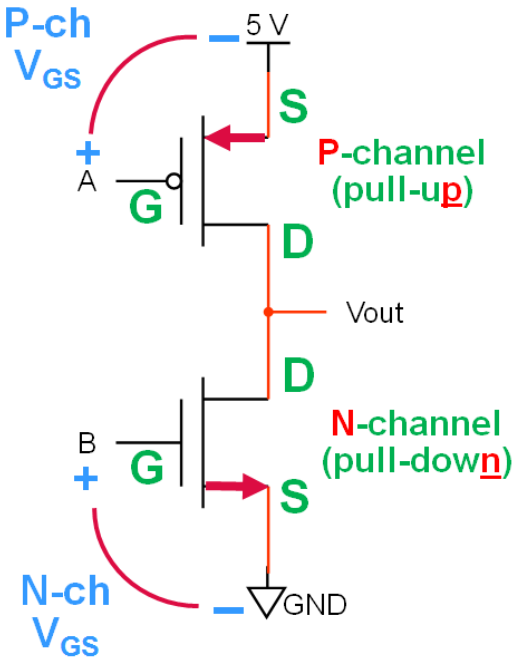
  - **N-channel MOS (NMOS)**



Voltage-controlled resistance:
increase V_{GS} → decrease R_{DS}
(current flows from D terminal to S)
Note: normally, $V_{GS} \geq 0$

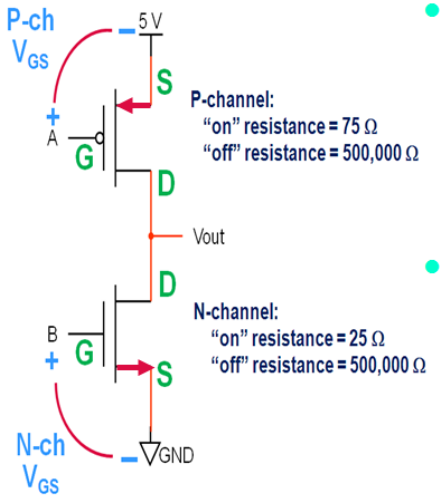
current only flows through the resistance *one way*

  - **basic CMOS logic circuit**



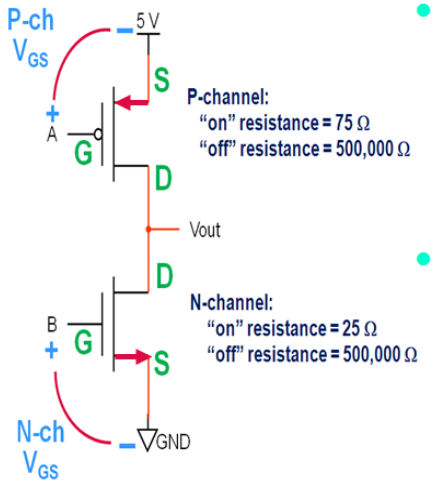
- The S terminal of the P-ch MOSFET is connected to 5 V
- The S terminal of the N-ch MOSFET is connected to GND
- The D terminals of both MOSFETs are connected to the output (Vout)
- The direction of current flow in the P-ch device is from the S terminal to the D terminal ("sources" current)
- The direction of current flow in the N-ch device is from the D terminal to the S terminal ("sinks" current)
- A high voltage on the G terminal of the N-ch MOSFET (relative to GND) turns it on
- A low voltage on the G terminal of the P-ch MOSFET (relative to 5 V) turns it on

- **example: inverter operation (very low power dissipation, very low voltage drop across "on" device under "no load" conditions)**



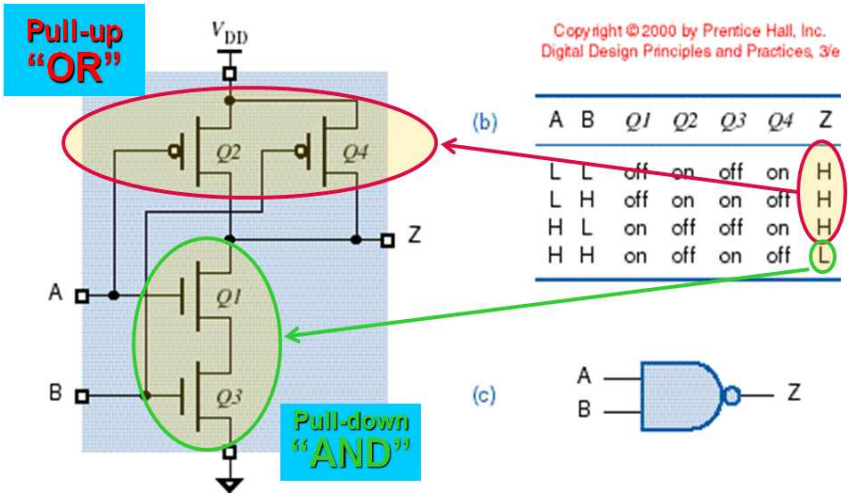
- Calculate V_{out} for the case A=B=0V
  - P-ch device is "on" (R_{DS} = 75 Ω)
  - N-ch device is "off" (R_{DS} = 500,000 Ω)
  - V_{out} = 5 x (500,000 / 500,075) ≈ 4.999 V
  - $P_{dissipation}$ = 5^2 / 500,075 ≈ 0.05 mW
- Calculate V_{out} for the case A=B=5V
  - P-ch device is "off" (R_{DS} = 500,000 Ω)
  - N-ch device is "on" (R_{DS} = 25 Ω)
  - V_{out} = 5 x (25 / 500,025) ≈ 0.00025 V
  - $P_{dissipation}$ = 5^2 / 500,025 ≈ 0.05 mW

- **example: "non-inverter" operation (Q: what would you call each of these cases?)**



- Calculate V_{out} for the case A=0, B=5 V
  - P-ch device is "on" (R_{DS} = 75 Ω)
  - N-ch device is "on" (R_{DS} = 25 Ω)
  - V_{out} = 5 x (25 / 100) = 1.25 V
  - $P_{dissipation}$ = 5^2 / 100 = 250 mW
- Calculate V_{out} for the case A=5V, B=0
  - P-ch device is "off" (R_{DS} = 500,000 Ω)
  - N-ch device is "off" (R_{DS} = 500,000 Ω)
  - V_{out} = 5 x (500,000 / 1,000,000) = 2.5 V
  - $P_{dissipation}$ = 5^2 / 1,000,000 = 0.025 mW

- **basic CMOS NAND gate**



more input combinations pull output high than low → P-channel pull-ups in *parallel* ("OR"), N-channel pull-downs in *series* ("AND")