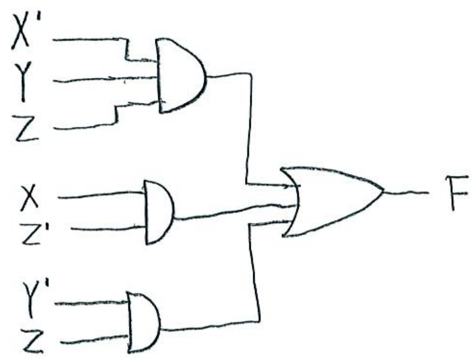
Huddle Board Exercise for Module 2 – No. 1
Monday, February 17, 2014

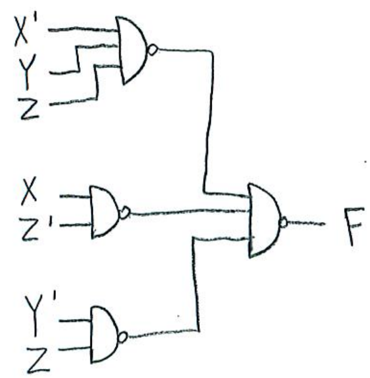
Draw the **AND-OR** realization and the **NAND-NAND** realization of the following function:

$$F(X,Y,Z) = X'\cdot Y\cdot Z + X\cdot Z' + Y'\cdot Z$$



AND-OR

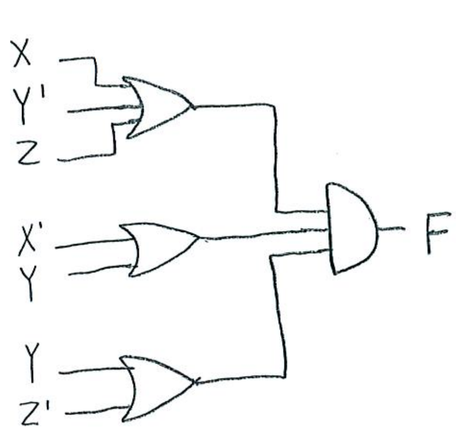
$\equiv$



NAND-NAND

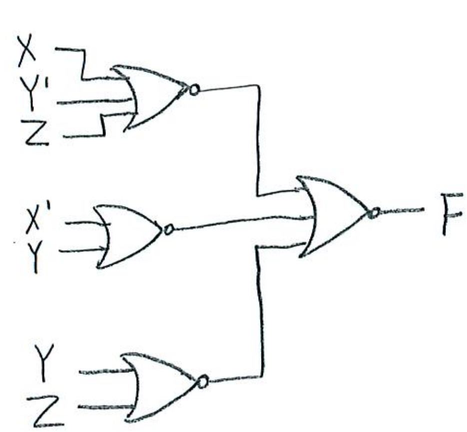
Draw the **OR-AND** realization and the **NOR-NOR** realization of the following function:

$$F(X,Y,Z) = (X+Y'+Z)\cdot(X'+Y)\cdot(Y+Z')$$



OR-AND

$\equiv$



NOR-NOR

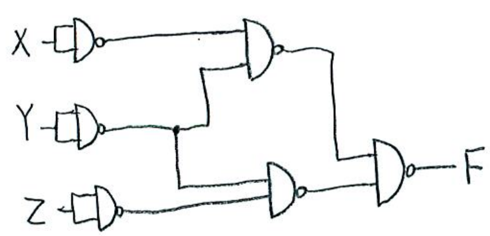
Huddle Board Exercise for Module 2 – No. 1a
Monday, February 17, 2014

1. **Assuming that *only true* variables are available, realize the function F(X,Y,Z) mapped below three different ways:**
   - **(a) Using only 7400 (quad 2-input NAND) chips**
   - **(b) Using only 7402 (quad 2-input NOR) chips**
   - **(c) Using only 7403 (quad 2-input open-drain NAND) chips**

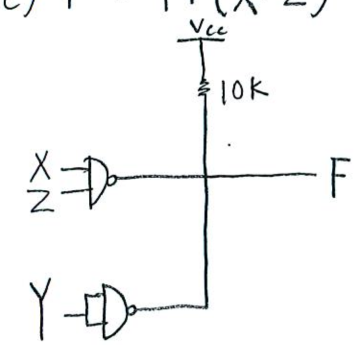
	X′		X	
Z′	1	d	0	1
Z	1	0	0	0
	Y′	Y	Y	Y′

Show complete schematics for each realization, along with your derivations.

(a) $F = X' \cdot Y' + Y' \cdot Z'$

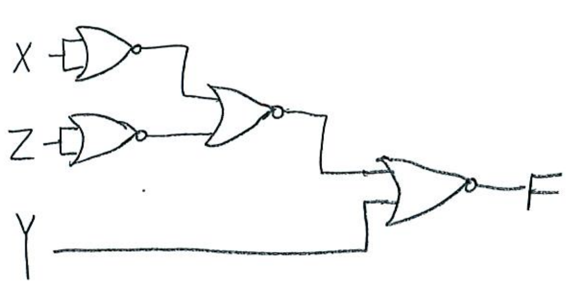


(c) $F' = Y + (X \cdot Z)$

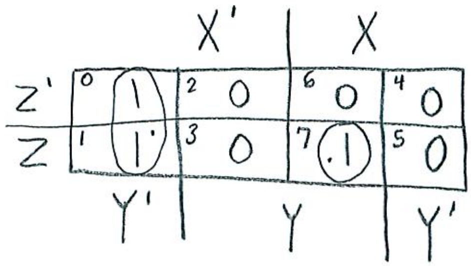


(b) $F' = Y + (X \cdot Z)$

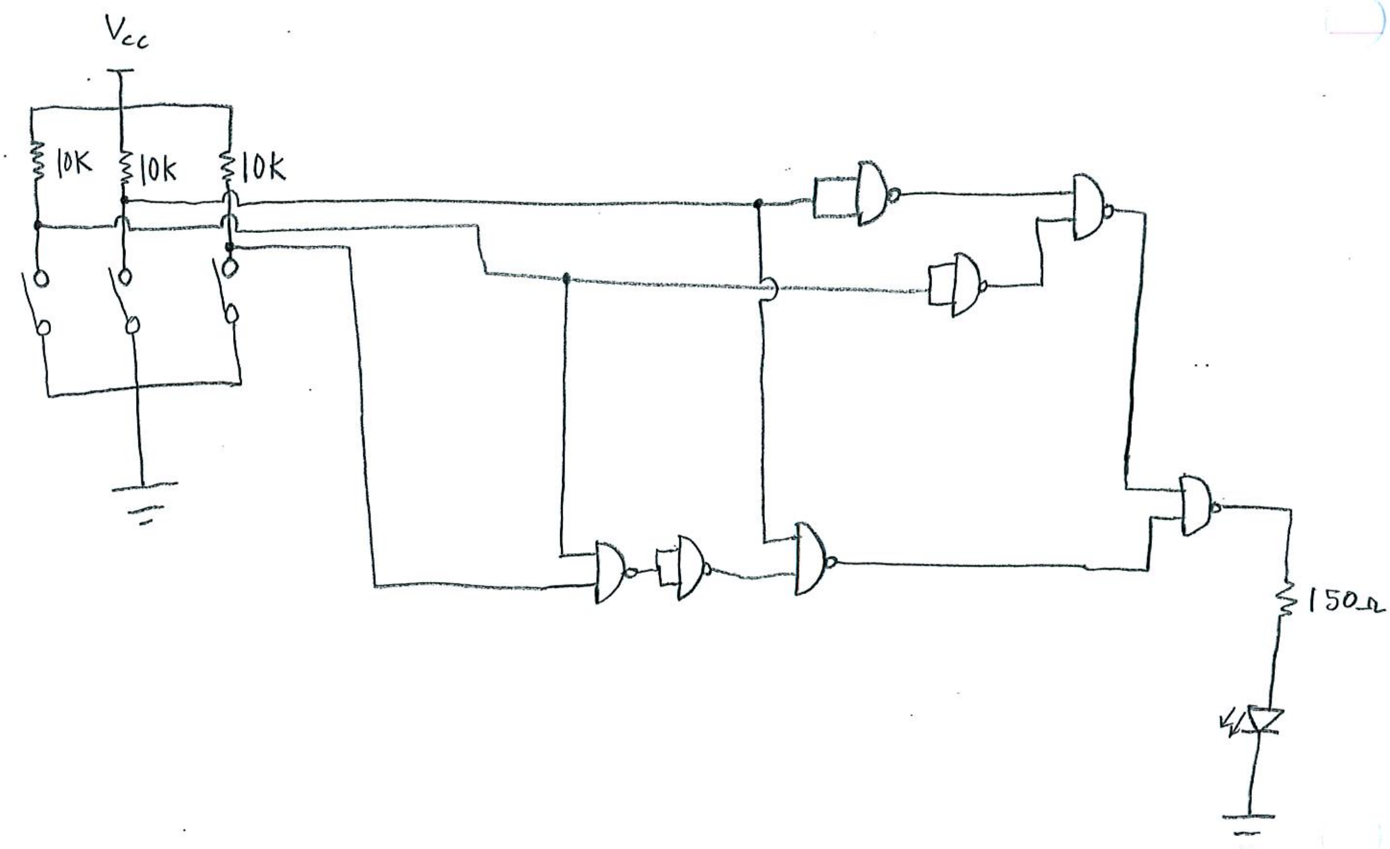
$F = Y' \cdot (X' + Z')$



2. Equipped only with a bucket full of 2-input NAND gates (plus a breadboard, some wires, some SPST switches, an LED, some resistors, and a power supply), you must implement the function represented by the ON SET $\Sigma_{X,Y,Z}(0,1,7)$ as efficiently and quickly as possible. ***Show all of your work, plus a <u>complete</u> schematic (including the switches, resistors, LED, and however many 2-input NAND gates deemed necessary).***



$$F = X' \cdot Y' + X \cdot Y \cdot Z$$



Huddle Board Exercise for Module 2 – No. 1b
Monday, February 17, 2014

Practice for standardized exam questions — determine the <u>one</u> best response.

The following K-map applies to questions 1 through 6:

	X'		X	
Z'	1	1	0	d
Z	0	0	1	0
	Y'	Y		Y'

$F = X' \cdot Z' + X \cdot Y \cdot Z$

$F' = X \cdot Z' + X' \cdot Z + Y' \cdot Z$

$F = (X' + Z) \cdot (X + Z') \cdot (Y + Z')$

1. Assuming the availability of **only true** input variables, the **fewest number of 2-input NAND gates** that are needed to realize this function is:

   (A) 6 (B) 7 (C) 8 (D) 9 (E) none of the above

2. Assuming the availability of **only true** input variables, the **fewest number of 2-input NOR gates** that are needed to realize this function is:

   (A) 6 (B) 7 (C) 8 (D) 9 (E) none of the above

3. Assuming the availability of **only true** input variables, the **fewest number of 2-input open-drain NAND gates** that are needed to realize this function is:

   (A) 6 (B) 7 (C) 8 (D) 9 (E) none of the above

4. The **number of pull-up resistors** required for realizing this function as described in **question 3, above,** is:

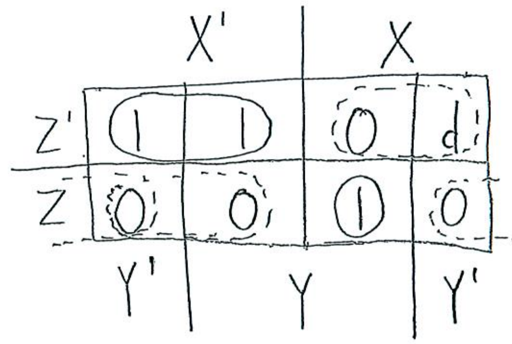
   (A) 1 (B) 2 (C) 3 (D) 4 (E) none of the above

5. The **cost** of a **minimal sum of products** realization of this function (assuming **<u>both</u> true and complemented variables** are available) would be:

   (A) 9 (B) 10 (C) 11 (D) 12 (E) none of the above

6. The **cost** of a **minimal products of sum** realization of this function (assuming **<u>both</u> true and complemented variables** are available) would be:

   (A) 9 (B) 10 (C) 11 (D) 12 (E) none of the above

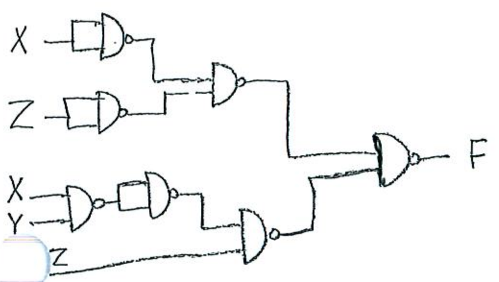


$F = X' \cdot Z' + X \cdot Y \cdot Z$ $F' = X \cdot Z' + X' \cdot Z + Y' \cdot Z$ $F = (X'+Z) \cdot (X+Z') \cdot (Y+Z')$

① Fewest number of 2-input NAND gates

$F = X' \cdot Z' + X \cdot Y \cdot Z$

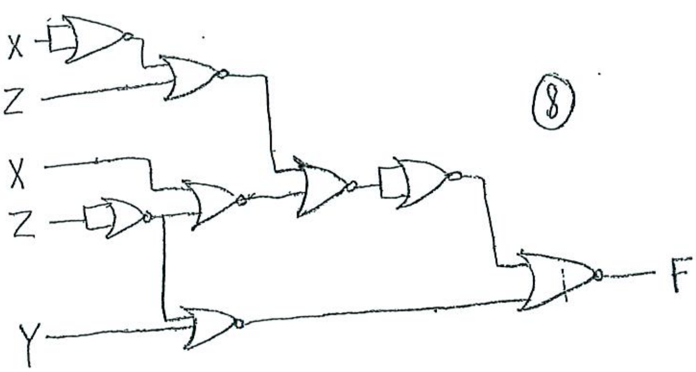
⑦



② Fewest number of 2-input NOR gates

$F = (X'+Z) \cdot (X+Z') \cdot (Y+Z')$

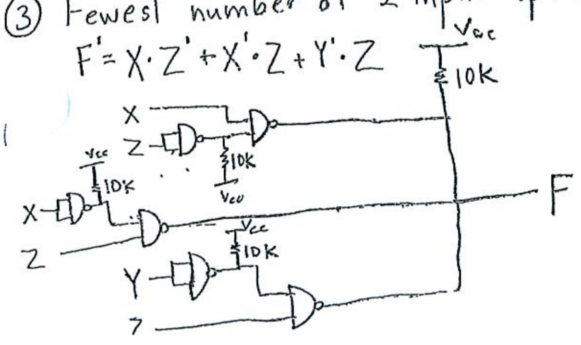
⑧



③ Fewest number of 2-input open-drain NAND gates

$F' = X \cdot Z' + X' \cdot Z + Y' \cdot Z$

⑥

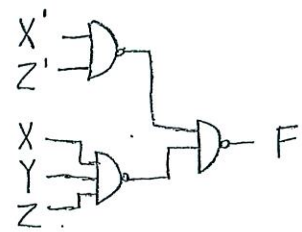


④ Number of pull-up resistors for open-drain NAND gates

4 pull-up resistors

⑤ Cost of minimal sum of products

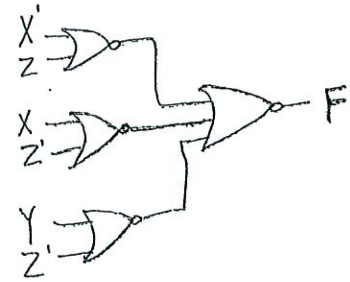
$F = X' \cdot Z' + X \cdot Y \cdot Z$



7 inputs + 3 outputs = 10

⑥ Cost of minimal product of sums

$F = (X'+Z) \cdot (X+Z') \cdot (Y+Z')$

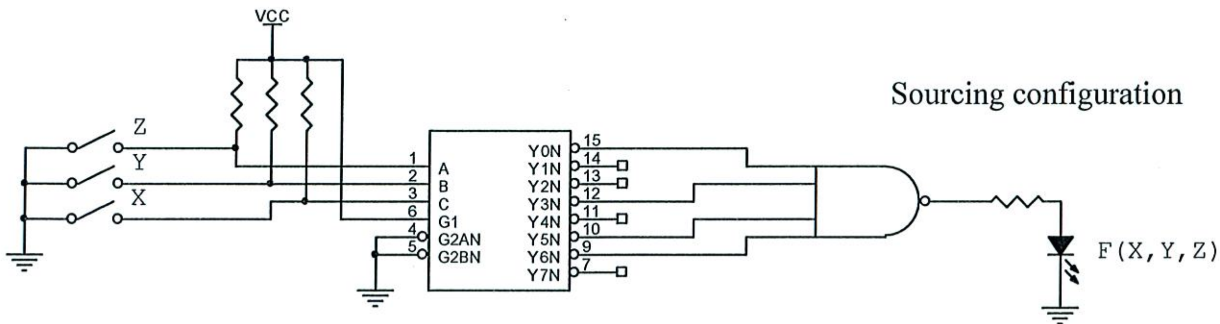


9 inputs + 4 outputs = 13

Huddle Board Exercise for Module 2 – No. 2
Wednesday, February 26, 2014

Determine the **ON set** and a simplified **minimum sum-of-products** function realized by this decoder-based circuit.

Sourcing configuration



Derivation:

	X′		X	
Z′	1	0	1	0
Z	0	1	0	1
	Y′	Y		Y′

$\Sigma_{X,Y,Z}$ **(0,3,5,6)**

$F = X'\bullet Y'\bullet Z' + X'\bullet Y\bullet Z + X\bullet Y\bullet Z' + X\bullet Y'\bullet Z$

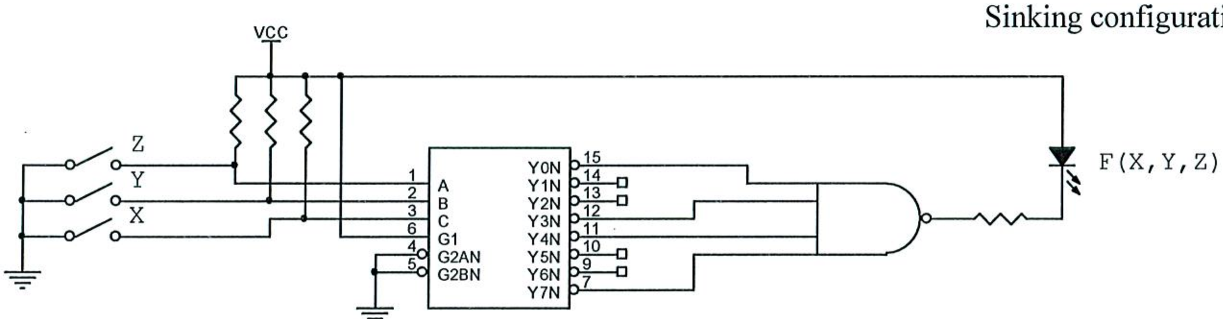
$= X'\bullet (Y'\bullet Z' + Y\bullet Z) + X\bullet (Y\bullet Z' + Y'\bullet Z)$

$= X'\bullet (Y \oplus Z)' + X\bullet (Y \oplus Z)$

Solutions will vary depending on which variable is factored out. There should be one XNOR and one XOR term.

Determine the **ON set** and a simplified **minimum sum-of-products** function realized by this decoder-based circuit.

Sinking configuration



Derivation:

	X′		X	
Z′	0	1	1	0
Z	1	0	0	1
	Y′	Y		Y′

$\Sigma_{X,Y,Z}$ **(1,2,5,6)**

$F = Y\bullet Z' + Y'\bullet Z$

$= Y \oplus Z$