Lecture Summary – Module 1

Switching Algebra and CMOS Logic Gates

Learning Outcome: ***an ability to analyze and design CMOS logic gates***

Learning Objectives:

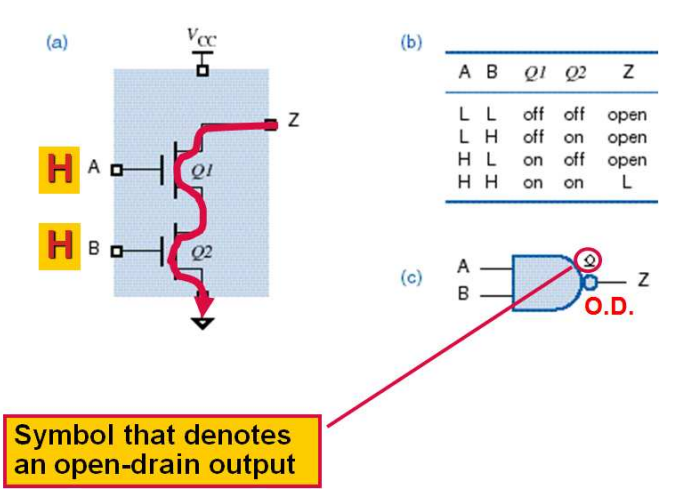
1-1. convert numbers from one base (radix) to another: 2, 10, 16
1-2. define a binary variable
1-3. identify the theorems and postulates of switching algebra
1-4. describe the principle of duality
1-5. describe how to form a complement function
1-6. prove the equivalence of two Boolean expressions using perfect induction
1-7. describe the function and utility of basic electronic components (resistors, capacitors, diodes, MOSFETs)
1-8. define the switching threshold of a logic gate and identify the voltage ranges typically associated with a "logic high" and a "logic low"
1-9. define assertion level and describe the difference between a positive logic convention and a negative logic convention
1-10. describe the operation of basic logic gates (NOT, NAND, NOR) constructed using N- and P-channel MOSFETs and draw their circuit diagrams
1-11. define "fighting" among gate outputs wired together and describe its consequence
1-12. define logic gate fan-in and describe the basis for its practical limit
1-13. identify key information contained in a logic device data sheet
1-14. calculate the DC noise immunity margin of a logic circuit and describe the consequence of an insufficient margin
1-15. describe the consequences of a "non-ideal" voltage applied to a logic gate input
1-16. describe how unused ("spare") CMOS inputs should be terminated
1-17. describe the relationship between logic gate output voltage swing and current sourcing/sinking capability
1-18. describe the difference between "DC loads" and "CMOS loads"
1-19. calculate V_{OL} and V_{OH} of a logic gate based on the "on" resistance of the active device and the amount of current sourced/sunk by the gate output
1-20. calculate logic gate fan-out and identify a practical lower limit
1-21. calculate the value of current limiting resistor needed for driving an LED
1-22. describe the deleterious effects associated with loading a gate output beyond its rated specifications
1-23. define propagation delay and list the factors that contribute to it
1-24. define transition time and list the factors that contribute to it
1-25. estimate the transition time of a CMOS gate output based on the "on" resistance of the active device and the capacitive load
1-26. describe ways in which load capacitance can be minimized
1-27. identify sources of dynamic power dissipation
1-28. plot power dissipation of CMOS logic circuits as a function of operating frequency
1-29. plot power dissipation of CMOS logic circuits as a function of power supply voltage
1-30. describe the function and utility of decoupling capacitors
1-31. define hysteresis and describe the operation of Schmitt-trigger inputs
1-32. describe the operation and utility of a transmission gate
1-33. define high-impedance state and describe the operation of a tri-state buffer
1-34. define open drain as it applies to a CMOS logic gate output and calculate the value of pull-up resistor needed
1-35. describe how to create "wired logic" functions using open drain logic gates
1-36. calculate the value of pull-up resistor needed for an open drain logic gate

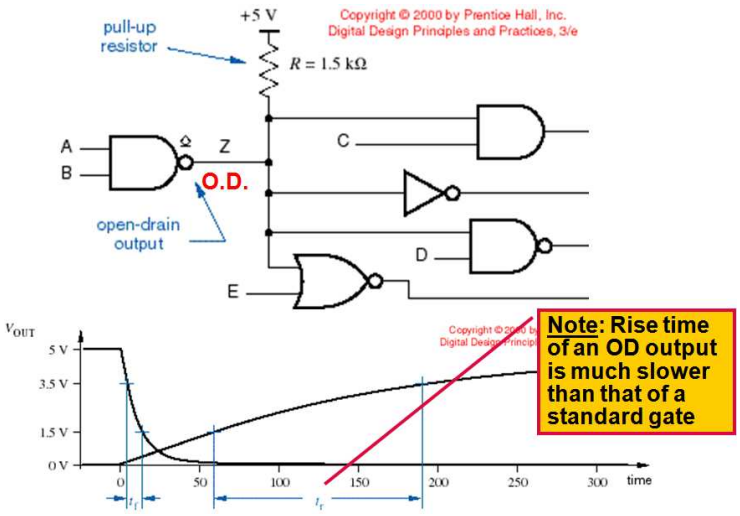
Lecture Summary – Module 1-J

Three-State and Open-Drain Outputs

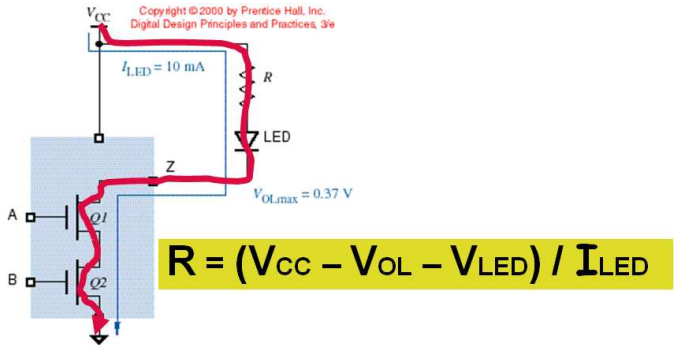
Reference: *Digital Design Principles and Practices* (4th Ed.), pp. 132-136, 138-141

- **open-drain outputs**
  - **<u>definition</u>: a CMOS output structure that does <u>not</u> include a P-channel (pull-up) transistor is called an *open-drain output***
  - **an open-drain output is in one of two states: LOW or "open" (i.e., disconnected)**
  - **an *underscored diamond* (or "O.D.") is used to indicate that an output is open drain**
  - **an open-drain output requires an external pull-up resistor to *passively* pull it high in the "open" state (since the output structure does NOT include a P-channel active pull-up)**

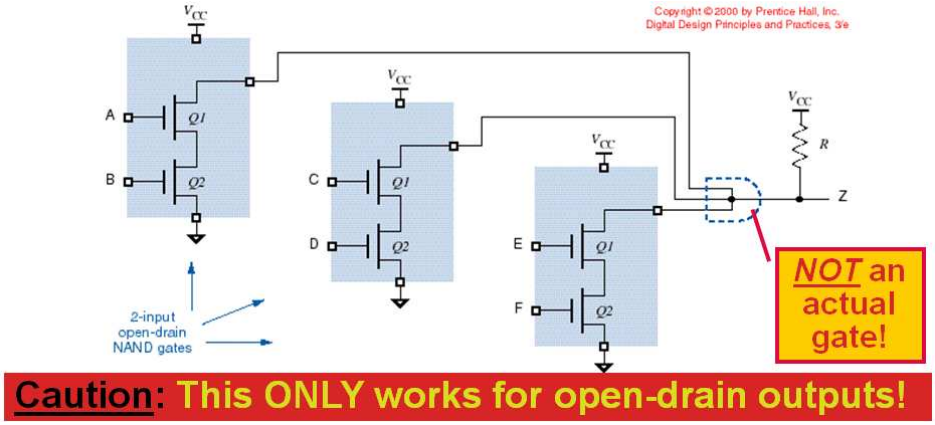




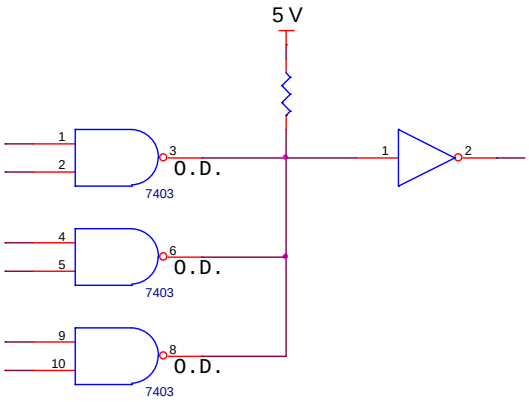
- **open-drain outputs, continued…**
  - **application – driving LEDs (O.D. outputs can typically sink more current than conventional gates)**



  - **application - "wired" logic (definition: *wired logic* is performed if the outputs of several open-drain gates are tied together with a single pull-up resistor)**

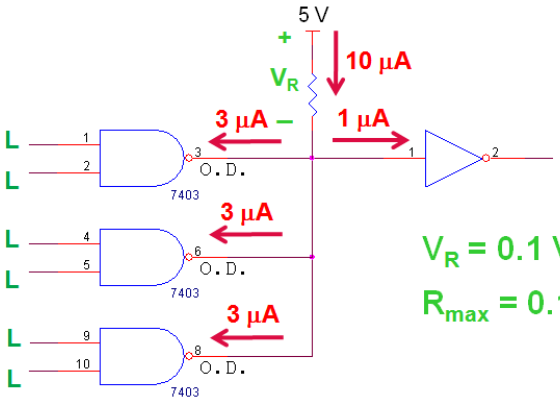


  - **pull-up resistor calculations**
    - **in open-drain applications, two calculations bracket the allowable values of the pull-up resistor R:**
      - **LOW - the sum of the current through R plus the LOW state input currents of the gate inputs driven *must not exceed* the I_{OLmax} of the active device**
      - **HIGH - the voltage drop across R in the HIGH state *must not reduce* the output voltage below the V_{IHmin} of the driven gate inputs**
  - **example: calculate a suitable value of pull-up resistor to use with the following circuit:**



Specifications (hypothetical data):
- **Off-state leakage current of O.D. NAND gate output: +3 μA**
- **I_{IH} and I_{IL} required by inverter input: ±1 μA**
- **V_{IH} desired for inverter input: 4.9 V**
- **$I_{OL\ max}$ of O.D. NAND gate output: +10 mA @ V_{OL} = 0.3 V**

- **open-drain outputs, continued…**
  - **pull-up resistor calculation example, continued…**
    - **solution, <u>maximum</u> R Value – based on V_{IH} desired**



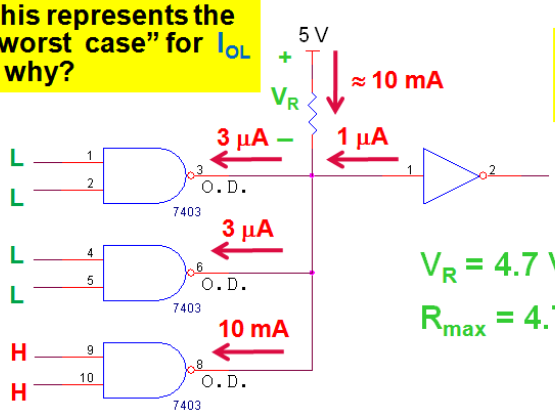
Conclusion – A pull-up resistor ranging from 470 Ω (R_{min}) to 10,000 Ω (R_{max}) will satisfy the specified constraints

$V_R = 0.1$ V $I_R = 10$ µA

$R_{max} = 0.1/0.00001 = 10{,}000\ \Omega$

- **solution, <u>minimum</u> R Value – based on $I_{OL\ max}$ of <u>one</u> gate**

This represents the "worst case" for I_{OL} – why?



Here, can safely ignore leakage and I_{IL} currents – why?

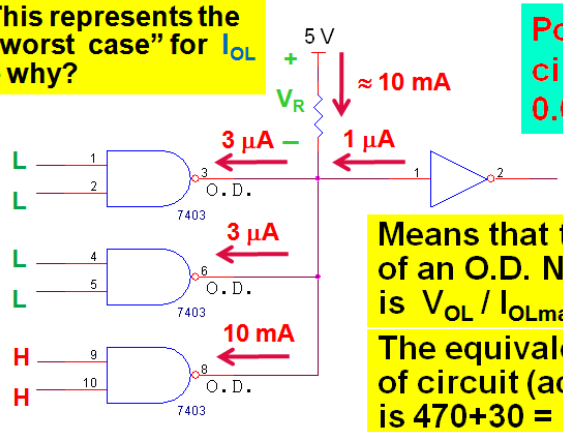
$V_R = 4.7$ V $I_R \approx 10$ mA

$R_{max} = 4.7/0.01 = 470\ \Omega$

NOTE: Picking R_{min} will minimize the rise time, while picking R_{max} will minimize the power dissipation

- **"prove" the "worst case" scenario (R = 470 Ω)**

This represents the "worst case" for I_{OL} – why?



Power dissipation of circuit is $I_R^2 \times R_{eq} = 0.01^2 \times 500 \approx 50$ mW

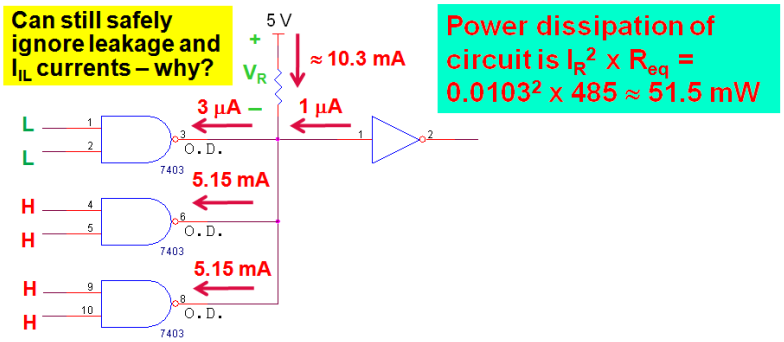
Means that the "on" resistance of an O.D. NAND gate used here is $V_{OL} / I_{OLmax} = 0.3/0.01 = 30\ \Omega$

The equivalent load impedance of circuit (across power supply) is $470+30 = 500\ \Omega$

Specifications (hypothetical data):

- Off-state leakage current of O.D. NAND gate output: +3 µA
- I_{IH} and I_{IL} required by inverter input: ±1 µA
- V_{IH} desired for inverter input: 4.9 V
- $I_{OL\ max}$ of O.D. NAND gate output: +10 mA @ $V_{OL} = 0.3$ V

- **open-drain outputs, continued…**
  - **pull-up resistor calculation example, continued…**
    - **"proof", continued…**

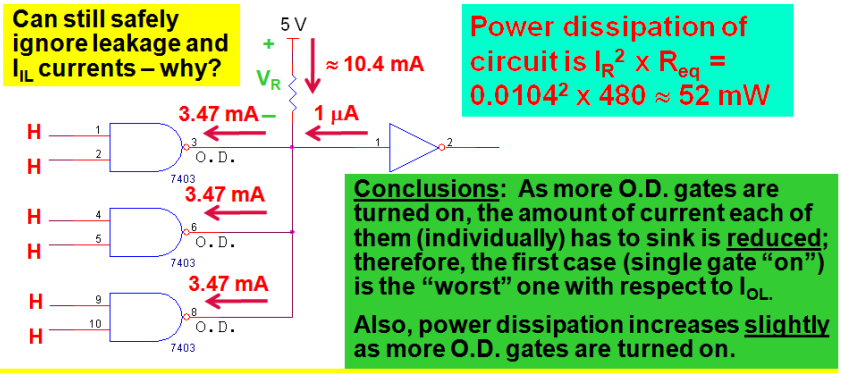


Next, turn on two O.D. gates

The equivalent load impedance of circuit is 470+15 = 485 Ω (because have two 30 Ω "on" resistances in parallel)

I_R is now 5 / 485 = 0.0103 A = 10.3 mA, which is split between the two gates that are "on"

    - **conclusions**



Conclusions: As more O.D. gates are turned on, the amount of current each of them (individually) has to sink is reduced; therefore, the first case (single gate "on") is the "worst" one with respect to I_{OL}.

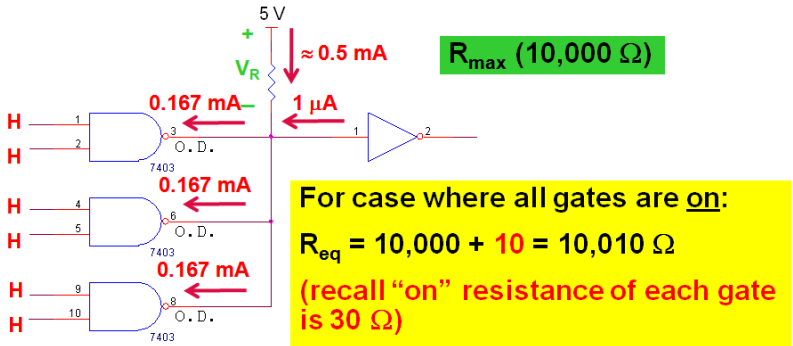
Also, power dissipation increases slightly as more O.D. gates are turned on.

Finally, turn on all three O.D. gates

The equivalent load impedance of circuit is 470+10 = 480 Ω (because have three 30 Ω "on" resistances in parallel)

I_R is now 5 / 480 = 0.0104 A = 10.4 mA, which is split among the three gates that are "on"

    - **compare power dissipation of circuit using R_{min} vs. R_{max} as the pull-up resistor**



Note: V_{IL} of inverter is nearly 0 V

For case where all gates are on:

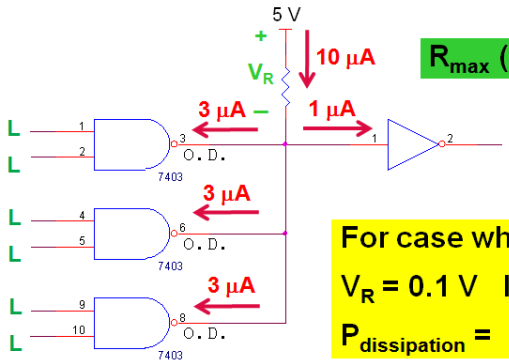
R_{eq} = 10,000 + 10 = 10,010 Ω

(recall "on" resistance of each gate is 30 Ω)

I_R ≈ 5 / 10,010 ≈ 0.5 mA (note - split among three gate outputs)

$P_{dissipation}$ = I_R^2 x R_{eq} ≈ 2.5 mW

- **open-drain outputs, continued…**
  - **pull-up resistor calculation example, continued…**
    - **power dissipation comparison, continued…**



R_{max} (10,000 Ω)

For case where all gates are off:

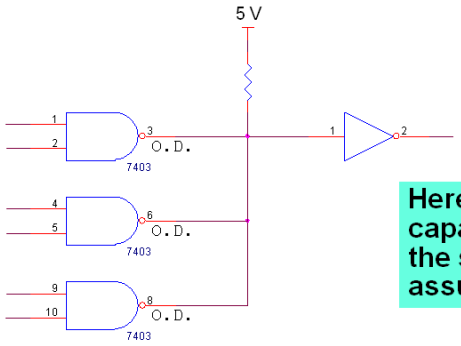
V_R = 0.1 V I_R = 10 μA

$P_{dissipation}$ = I_R^2 x R = 1 μW

Note: V_{IH} of inverter is 4.9 V

Conclusion: Power dissipation when R_{max} is used does not exceed 2.5 mW (vs. 52 mW for R_{min}); therefore, use of R_{max} minimizes the power dissipation

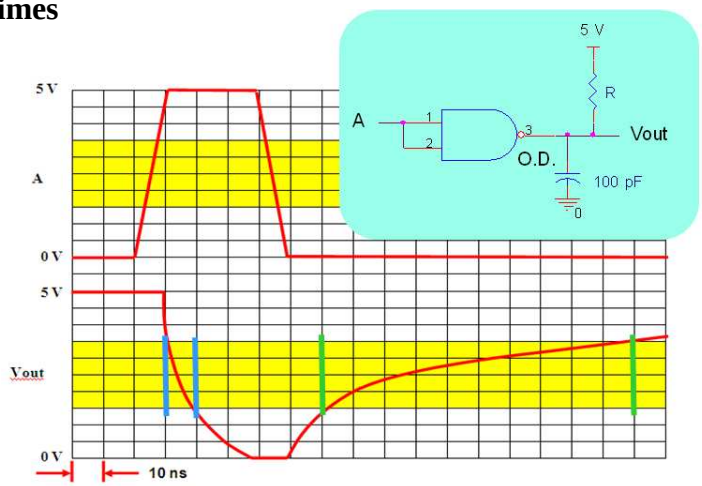
    - **compare rise time estimates of circuit using R_{min} vs. R_{max} as the pull-up resistor**



Here, need to know the capacitive load (C_L); for the sake of analysis, assume it is 100 pF

Comparison:
- For R_{min}, rise time estimate is 470 x 100 x 10^{-12} = 47 ns
- For R_{max}, rise time estimate is 10,000 x 100 x 10^{-12} = 1000 ns
- Conclusion: rise time for R_{max} case is considerably longer

  - **example: estimate the "on" resistance of an O.D. gate and pull-up resistor value based on rise/fall times**



rise time = 100 ns = $R_{pull\text{-}up}$ x 100 pF → $R_{pull\text{-}up}$ = 1000 Ω

fall time = 10 ns = R_{on} x 100 pF → R_{on} = 100Ω